

650V SuperGaN™ FET in TO-247 (source tab)

Ihr Vertriebspartner:



hy-line.de
LEADER IN TECHNOLOGY.

HY-LINE Power Components
Vertriebs GmbH
Inselkammerstr. 10
D-82008 Unterhaching
☎ +49 89 614 503 -10
power@hy-line.de

HY-LINE AG
Hochstrasse 355
CH-8200 Schaffhausen
☎ +41 52 647 42 00
info@hy-line.ch

Description

The TP65H015G5WS 650V, 15 mΩ gallium nitride GaN FET is a normally-off device using Transphorm's Gen V platform. It combines a state-of-the-art high voltage GaN HEMT with a low voltage silicon MOSFET to offer superior reliability and performance.

The Gen V SuperGaN™ platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge.

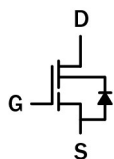
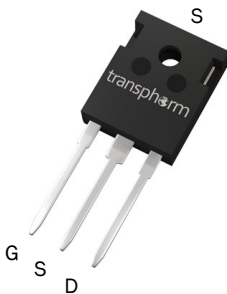
Related Literature

- [AN0009](#): Recommended External Circuitry for GaN FETs
- [AN0003](#): Printed Circuit Board Layout and Probing
- [AN0010](#): Paralleling GaN FETs

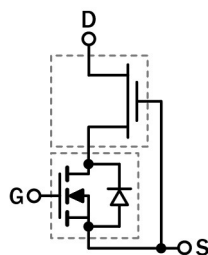
Ordering Information

Part Number	Package	Package Configuration
TP65H015G5WS	3 lead TO-247	Source

TP65H015G5WS
TO-247
(top view)



Cascade Schematic Symbol



Cascade Device Structure

Features

- JEDEC qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
 - Intrinsic lifetime tests
 - Wide gate safety margin
 - Transient over-voltage capability
- Very low Q_{RR}
- Reduced crossover loss

Benefits

- Enables AC-DC bridgeless totem-pole PFC designs
 - Increased power density
 - Reduced system size and weight
 - Overall lower system cost
- Achieves increased efficiency in both hard- and soft-switched circuits
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

Applications

- Datacom
- Broad industrial
- PV inverter
- Servo motor



Key Specifications

V_{DSS} (V)	650
$V_{(TR)DSS}$ (V)	725
$R_{DS(on)eff}$ (mΩ) max*	18
Q_{RR} (nC) typ	430
Q_G (nC) typ	68

* Dynamic on-resistance; see Figures 18 and 19

TP65H015G5WS-Preliminary

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise stated.)

Symbol	Parameter	Limit Value	Unit	
V_{DSS}	Drain to source voltage ($T_J = -55^\circ\text{C}$ to 150°C)	650	V	
$V_{(TR)DSS}$	Transient drain to source voltage ^a	725		
V_{GSS}	Gate to source voltage	± 20		
P_D	Maximum power dissipation @ $T_c=25^\circ\text{C}$	276	W	
I_D	Continuous drain current @ $T_c=25^\circ\text{C}$ ^b	95	A	
	Continuous drain current @ $T_c=100^\circ\text{C}$ ^b	60	A	
I_{DM}	Pulsed drain current (pulse width: $10\mu\text{s}$)	600	A	
T_c	Operating temperature	Case	-55 to $+150$	$^\circ\text{C}$
T_J		Junction	-55 to $+150$	$^\circ\text{C}$
T_S	Storage temperature	-55 to $+150$	$^\circ\text{C}$	
T_{SOLD}	Soldering peak temperature ^c	260	$^\circ\text{C}$	

Notes:

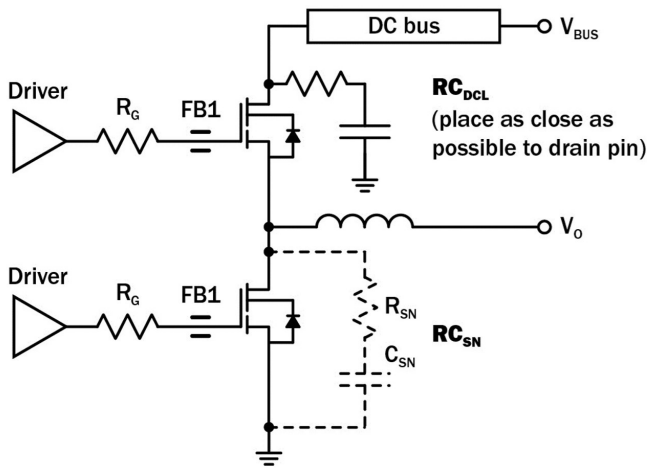
- In off-state, spike duty cycle $D < 0.01$, spike duration $< 1\mu\text{s}$
- For increased stability at high current operation, see Circuit Implementation on page 3
- For 10 sec., 1.6mm from the case

Thermal Resistance

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Junction-to-case	0.45	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient	40	$^\circ\text{C}/\text{W}$

TP65H015G5WS-Preliminary

Circuit Implementation



Layout Recommendations: (See also [AN0009](#))

Gate Loop:

- Gate Driver: SiLab Si823x/Si827x
- Keep gate loop compact
- Minimize coupling with power loop

Power loop: (For reference see page [13](#))

- Minimize power loop path inductance
- Minimize switching node coupling with high and low power plane
- Add DC bus snubber to reduce to voltage ringing
- Add Switching node snubber for high current operation

Simplified Half-bridge Schematic (See also on Figure [13](#))

Recommended gate drive: (0V, 12V) with $R_G=15\Omega$

Gate Ferrite Bead (FB1)	Required DC Link RC Snubber (RC_{DCL}) ^a	Recommended Switching Node RC Snubber (RC_{SN}) ^{b,c}
80-120 Ω at 100MHz	$[10nF + 3.3 \Omega] \times 3$	Not necessary

Notes:

- RC_{DCL} should be placed as close as possible to the drain pin
- RC_{SN} is needed only if R_G is smaller than recommendations or operational current exceeds 100C rated I_{DMAX}
- If required, please use (100 pF + 10 ohm) or parallel two or three of the same

TP65H015G5WS-Preliminary

Electrical Parameters (T_J=25 °C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
V _{(BL)DSS}	Drain-source voltage	650	—	—	V	V _{GS} =0V
V _{GS(th)}	Gate threshold voltage	3.3	4	4.8	V	V _{DS} =V _{GS} , I _D =2mA
R _{DS(on)eff}	Drain-source on-resistance ^a	—	15	18	mΩ	V _{GS} =10V, I _D =60A
		—	31	—		V _{GS} =10V, I _D =60A, T _J =150 °C
I _{DSS}	Drain-to-source leakage current	—	7	70	μA	V _{DS} =650V, V _{GS} =0V
		—	50	—		V _{DS} =650V, V _{GS} =0V, T _J =150 °C
I _{GSS}	Gate-to-source forward leakage current	—	—	400	nA	V _{GS} =20V
	Gate-to-source reverse leakage current	—	—	-400		V _{GS} =-20V
C _{ISS}	Input capacitance	—	4670	—	pF	V _{GS} =0V, V _{DS} =400V, f=1MHz
C _{OSS}	Output capacitance	—	312	—		
C _{RSS}	Reverse transfer capacitance	—	8	—		
C _{O(er)}	Output capacitance, energy related ^b	—	497	—	pF	V _{GS} =0V, V _{DS} =0V to 400V
C _{O(tr)}	Output capacitance, time related ^c	—	1020	—		
Q _G	Total gate charge	—	68	100	nC	V _{DS} =400V, V _{GS} =0V to 10V, I _D =60A
Q _{GS}	Gate-source charge	—	30	—		
Q _{GD}	Gate-drain charge	—	18	—		
Q _{OSS}	Output charge	—	430	—	nC	V _{GS} =0V, V _{DS} =0V to 400V
t _{D(on)}	Turn-on delay	—	78	—	ns	V _{DS} =400V, V _{GS} =0V to 12V, R _G =15Ω, Z _{FB} =120Ω at 100MHz, I _D =60A
t _R	Rise time	—	20	—		
t _{D(off)}	Turn-off delay	—	132	—		
t _F	Fall time	—	10	—		

Notes:

- Dynamic on-resistance; see Figures 18 and 19 for test circuit and conditions
- Equivalent capacitance to give same stored energy as V_{DS} rises from 0V to 400V
- Equivalent capacitance to give same charging time as V_{DS} rises from 0V to 400V

TP65H015G5WS-Preliminary

Electrical Parameters ($T_J=25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
I_S	Reverse current	—	—	60	A	$V_{GS}=0V$, $T_C=100^\circ\text{C}$ $\leq 15\%$ duty cycle
V_{SD}	Reverse voltage ^a	—	1.5	—	V	$V_{GS}=0V$, $I_S=60A$
		—	1.1	—		$V_{GS}=0V$, $I_S=30A$
t_{RR}	Reverse recovery time	—	100	—	ns	$I_S=60A$, $V_{DD}=400V$, $di/dt=1000A/\mu s$
Q_{RR}	Reverse recovery charge	—	430	—	nC	
$(di/dt)_{RM}$	Reverse diode di/dt ^b	—	—	3500	A/ μs	Circuit implementation and parameters on page 3

Notes:

- a. Includes dynamic $R_{DS(on)}$ effect
- b. Reverse conduction di/dt will not exceed this max value with recommended R_G .

TP65H015G5WS-Preliminary

Typical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise stated)

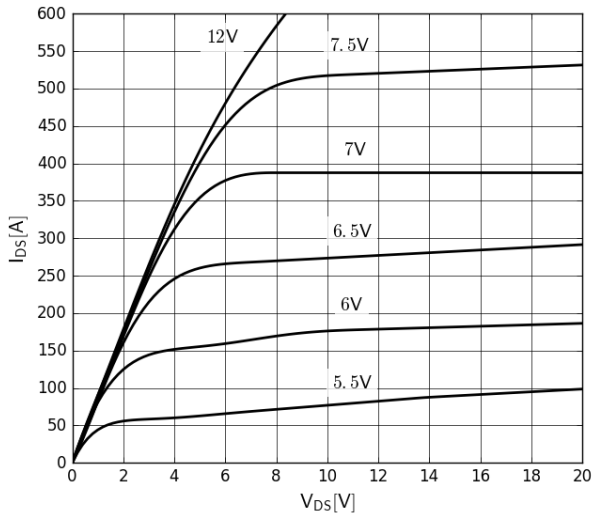


Figure 1. Typical Output Characteristics $T_J=25^\circ\text{C}$
Parameter: V_{GS}

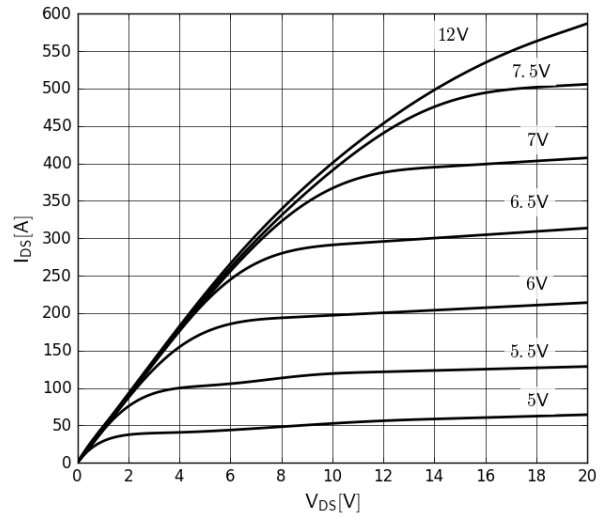


Figure 2. Typical Output Characteristics $T_J=150^\circ\text{C}$
Parameter: V_{GS}

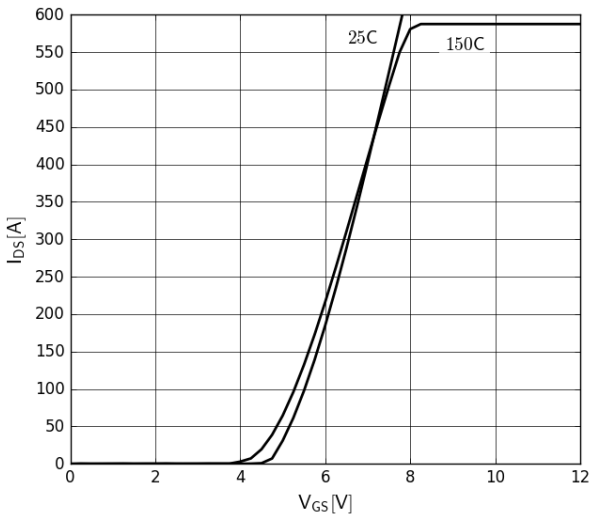


Figure 3. Typical Transfer Characteristics
 $V_{DS}=20\text{V}$, parameter: T_J

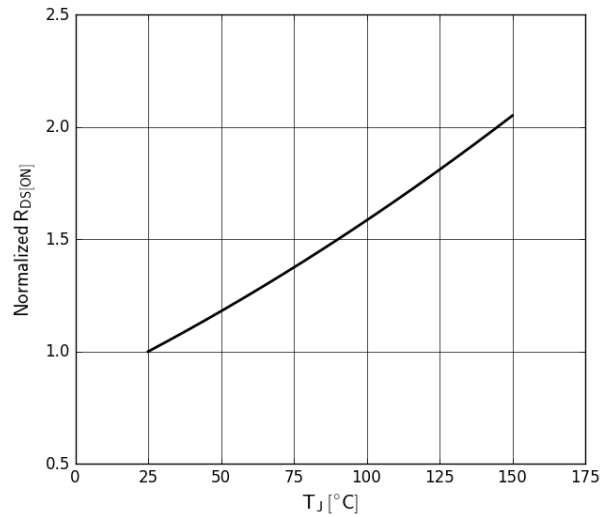


Figure 4. Normalized On-resistance
 $I_D=60\text{A}$, $V_{GS}=8\text{V}$

TP65H015G5WS-Preliminary

Typical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise stated)

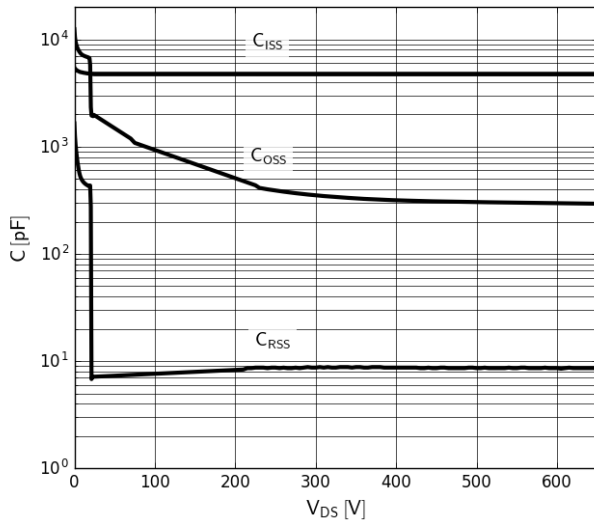


Figure 5. Typical Capacitance

$V_{GS}=0V$, $f=1\text{MHz}$

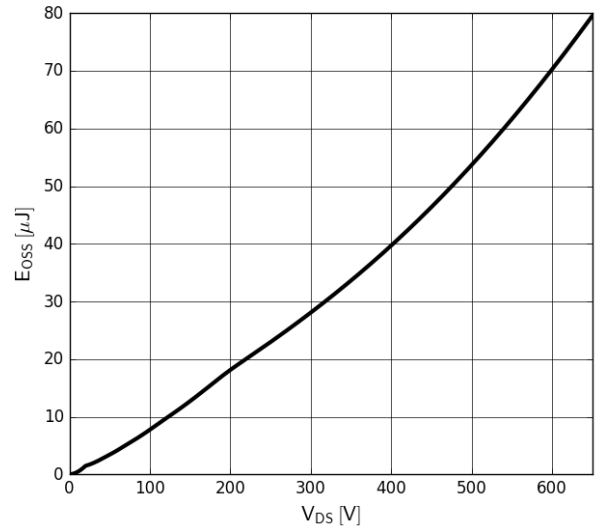


Figure 6. Typical C_{oss} Stored Energy

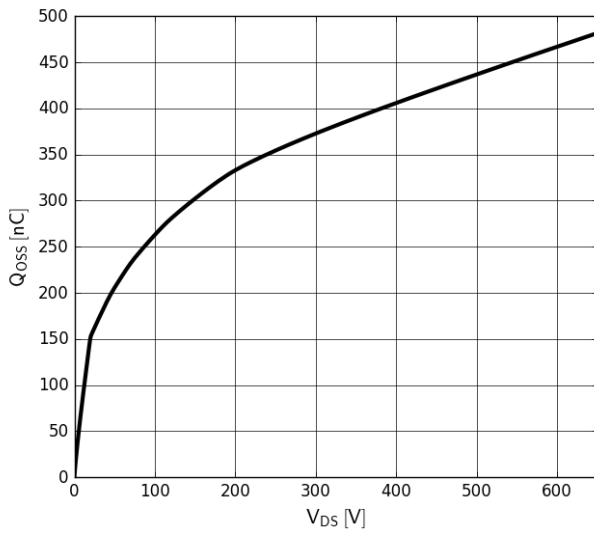


Figure 7. Typical Q_{oss}

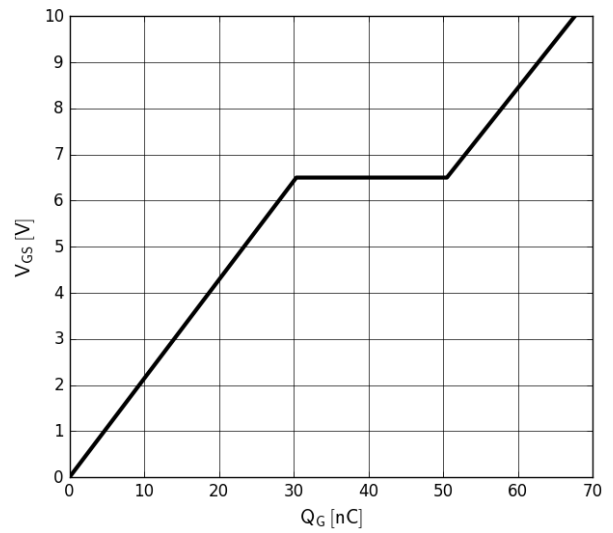


Figure 8. Typical Gate Charge

$I_{DS}=60A$, $V_{DS}=400V$

TP65H015G5WS-Preliminary

Typical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise stated)

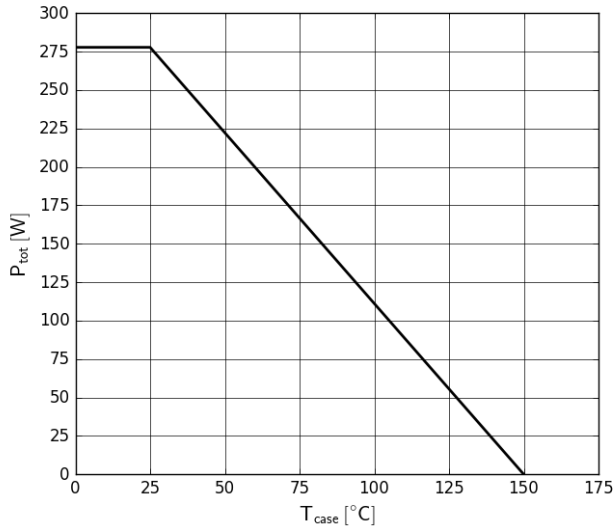


Figure 9. Power Dissipation

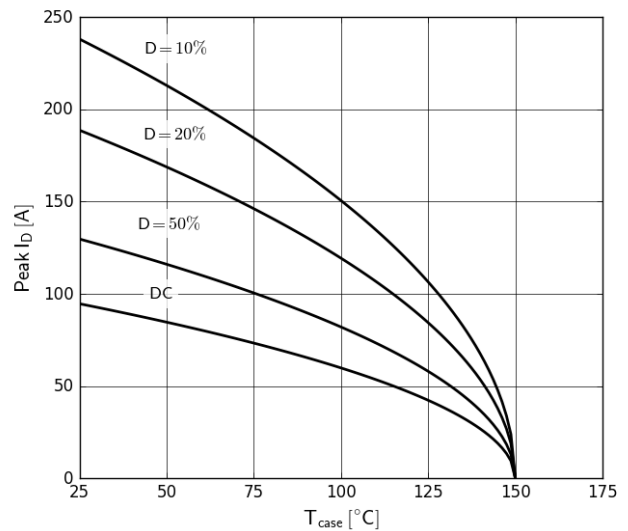


Figure 10. Current Derating
Pulse width $\leq 10\mu\text{s}$, $V_{GS} \geq 10\text{V}$

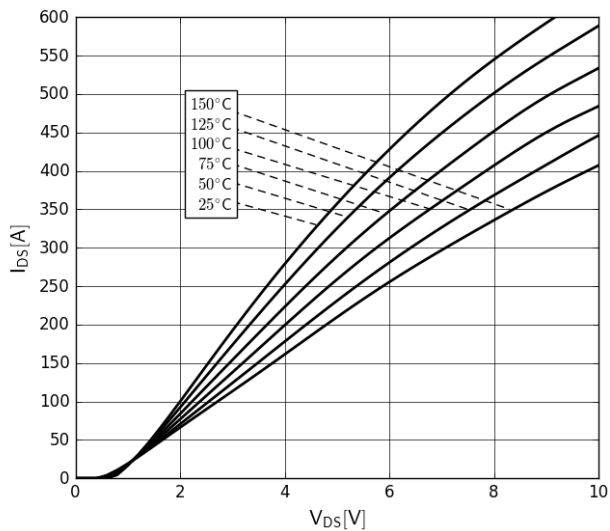


Figure 11. Forward Characteristics of Rev. Diode
 $I_S=f(V_{SD})$, parameter: T_J

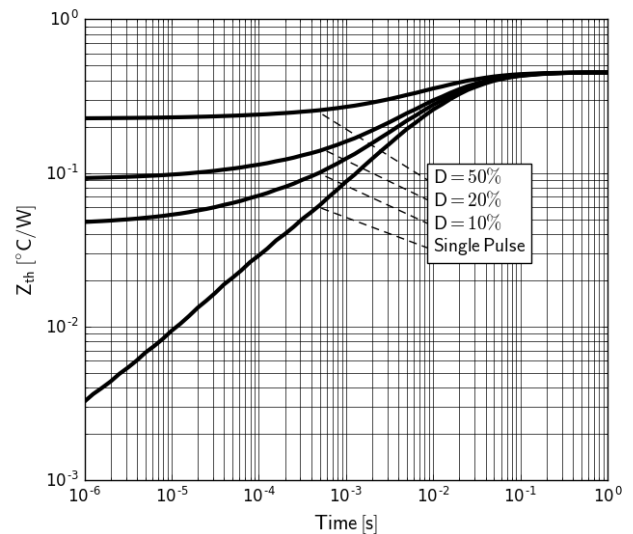


Figure 12. Transient Thermal Resistance

TP65H015G5WS-Preliminary

Typical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise stated)

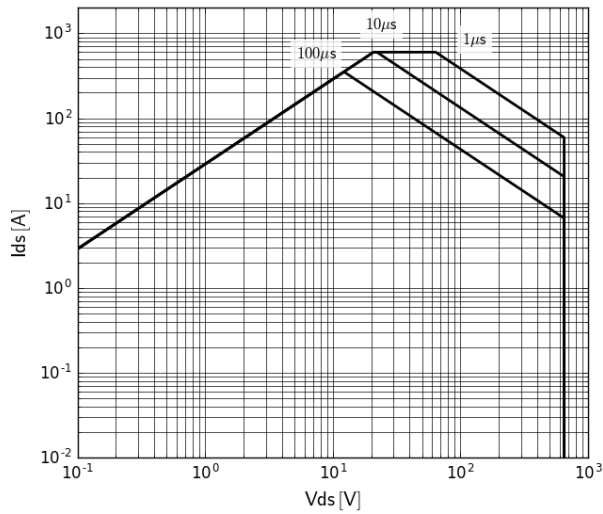


Figure 13. Safe Operating Area $T_C=25^\circ\text{C}$

TP65H015G5WS-Preliminary

Test Circuits and Waveforms

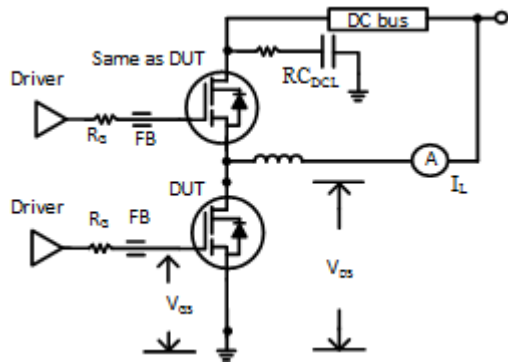


Figure 14. Switching Time Test Circuit
(see circuit implementation on page 3 for methods to ensure clean switching)

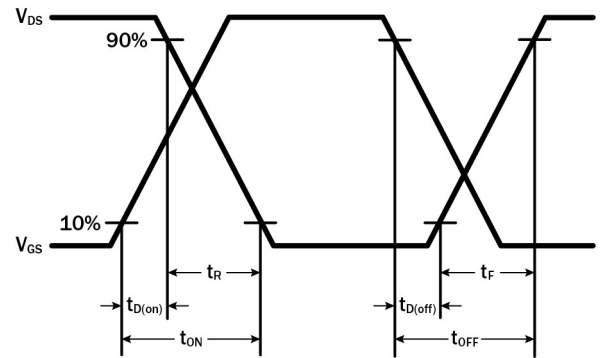


Figure 15. Switching Time Waveform

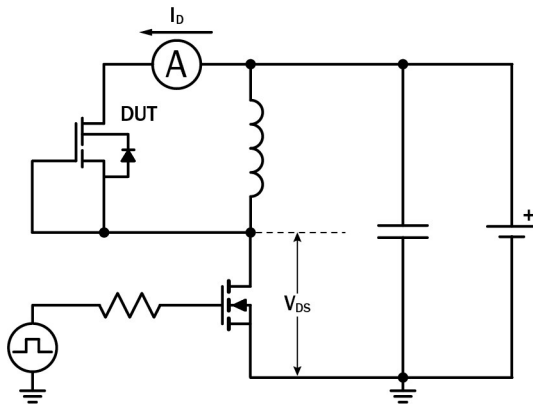


Figure 16. Diode Characteristics Test Circuit

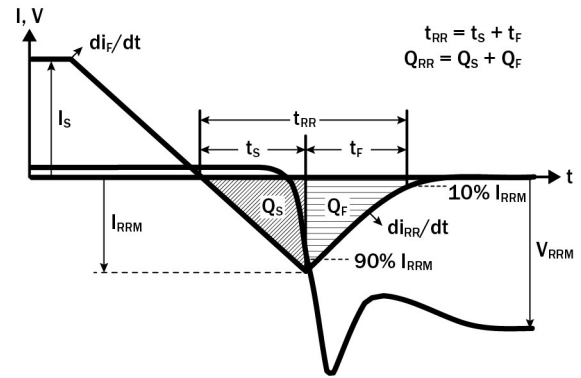


Figure 17. Diode Recovery Waveform

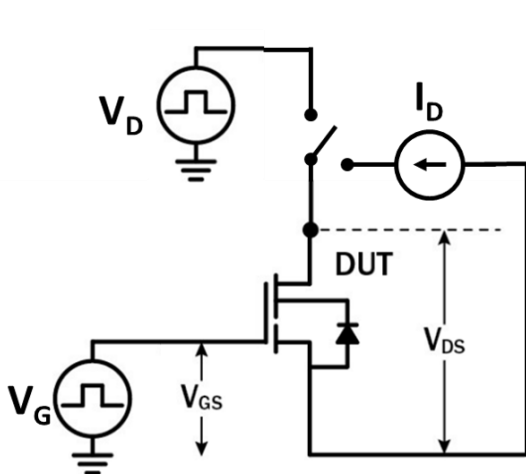


Figure 18. Dynamic $R_{DS(on)eff}$ Test Circuit

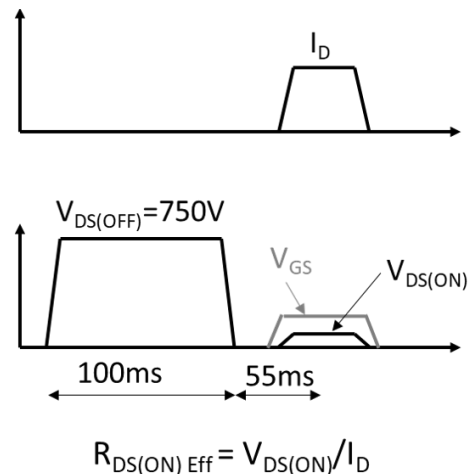


Figure 19. Dynamic $R_{DS(on)eff}$ Waveform

TP65H015G5WS-Preliminary

Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Transphorm GaN devices, see application note [Printed Circuit Board Layout and Probing for GaN Power Switches](#). The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Transphorm GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See AN0003 : Printed Circuit Board Layout and Probing	

GaN Design Resources

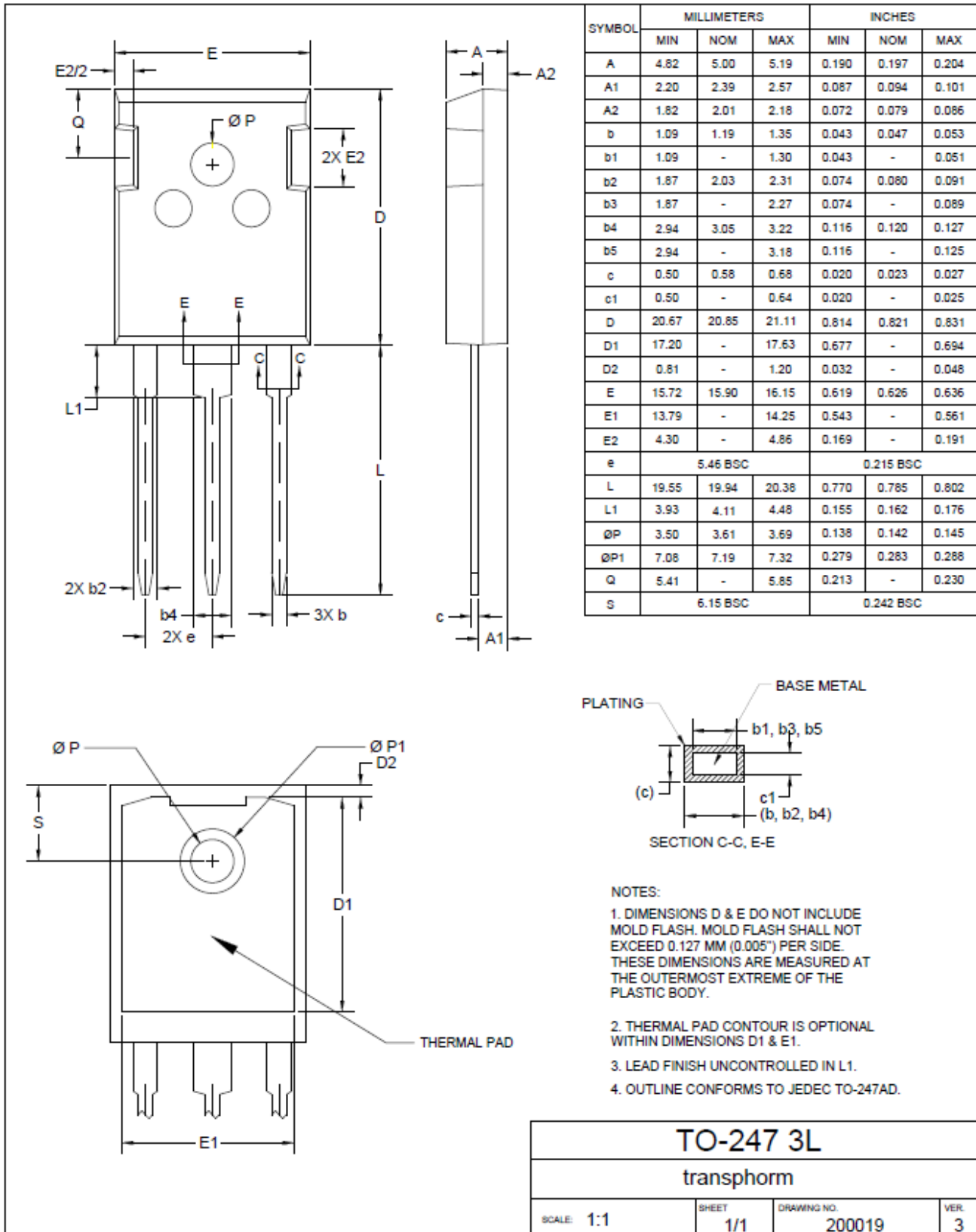
The complete technical library of GaN design tools can be found at transphormusa.com/design:

- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

TP65H015G5WS-Preliminary

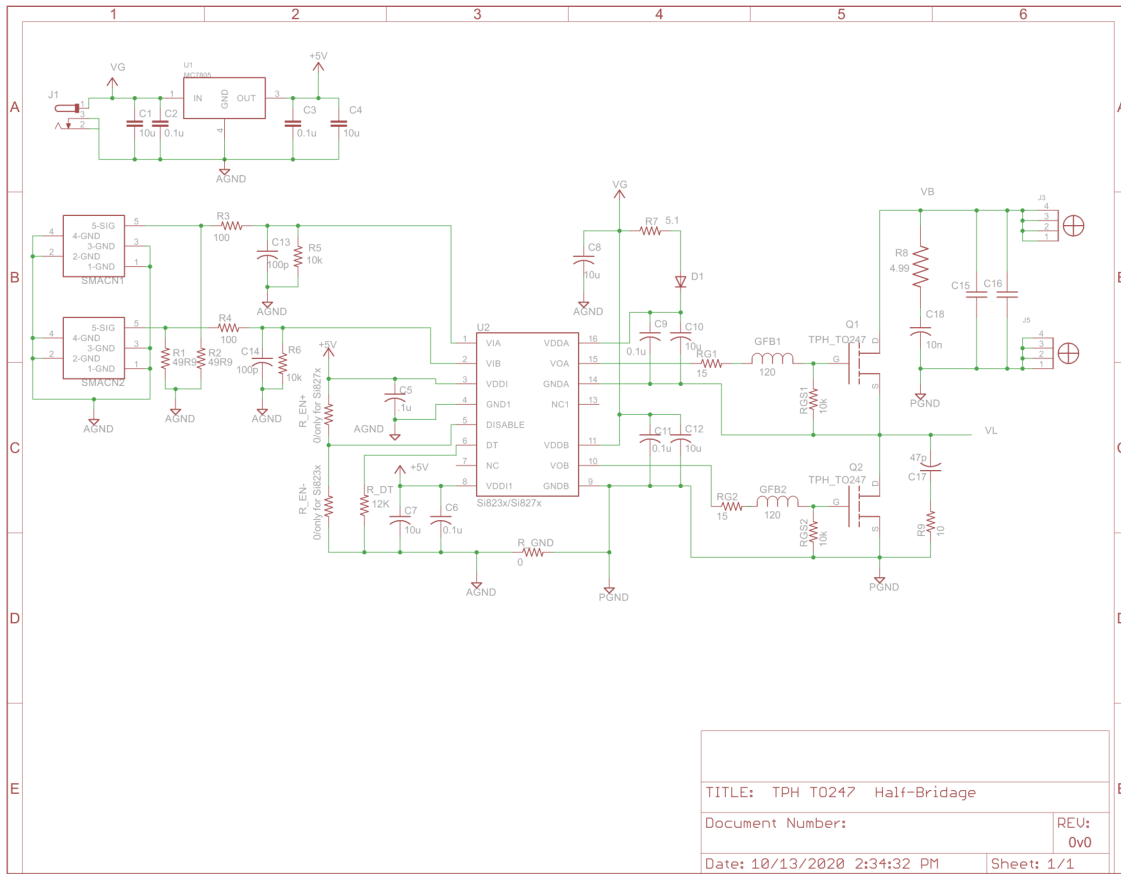
Mechanical

3 Lead TO-247 Package

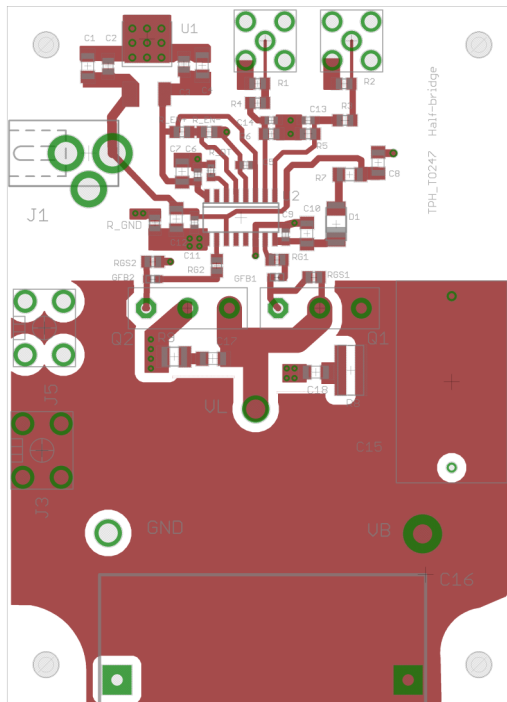


TP65H015G5WS-Preliminary

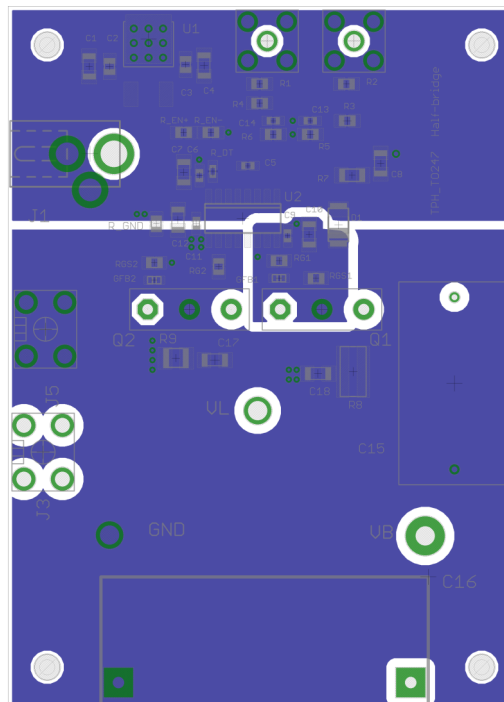
Half-bridge Reference Schematic and PCB Layout



Half-bridge layout Sample (Top Layer)



Half-bridge layout Sample (Bottom Layer)



TP65H015G5WS-Preliminary

Revision History

Version	Date	Change(s)
0.1	5/25/2020	Preliminary Datasheet
0.2	9/24/2020	Preliminary Datasheet
0.2	02/23/2021	Preliminary Datasheet. Update Figure 18, 19

Ihr Vertriebspartner:



HY-LINE Power Components
Vertriebs GmbH
Inselkammerstr. 10
D-82008 Unterhaching
☎ +49 89/ 614 503 -10
power@hy-line.de

HY-LINE AG
Hochstrasse 355
CH-8200 Schaffhausen
☎ +41 52 647 42 00
info@hy-line.ch