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User Guide

TDTTP2500B066B_0V1: 2.5kW Bridge-less Totem-pole PFC Evaluation Board

Overview

This user guide describes the TDTTP2500B066B 2.5kW bridgeless totem-pole power factor correction (PFC) evaluation board. Very high efficiency single-phase AC-DC conversion is achieved with the TP65H050G4BS, a diode-free Gallium Nitride (GaN) FET bridge with low reverse-recovery charge. Using Transphorm GaN FETs in the fast-switching leg of the circuit and low-resistance MOSFETs in the slow-switching leg of the circuit results in improved performance and efficiency. For more information and complete design files, please visit transphormusa.com.

The TDTTP2500B066B-KIT is for evaluation purposes only.

NOTE: Always download and install the latest TDTTP2500B066B firmware on the MICROCHIP.COM website. Refer to the installation instructions on the TDTTP2500B066B firmware guide for installation instructions

The evaluation board is shown in Fig. 1.

Figure 1. TDTTP2500B066B 2.5kW totem-pole PFC evaluation board

Warning

This evaluation board is intended to demonstrate GaN FET technology and is for demonstration purposes only and no guarantees are made for standards compliance. There are areas of this evaluation board that have exposed access to hazardous high voltage levels. Exercise caution to avoid contact with those voltages. Also note that the evaluation board may retain high voltage temporarily after input power has been removed. Exercise caution when handling. When testing converters on an evaluation board, ensure adequate cooling. Apply cooling air with a fan blowing across the converter or across a heat sink attached to the converter. Monitor the converter temperature to ensure it does not exceed the maximum rated per the datasheet specification.

TDTTP2500B066B input/output specifications

Input Voltage: 85 Vac to 265 Vac, 47 Hz to 63 Hz

Input Current: 10.5 A (rms) : (1250W at 115 Vac, 2500W at 230 Vac)

Ambient temperature: < 50 C

Output Voltage: 387 Vdc +/- 5 Vdc

PWM Frequency: 66 kHz

Auxiliary Supply: 12Vdc for bias voltage

Power dissipation in the GaN FET is limited by the maximum junction temperature. Refer to the TP65H050G4BS datasheet

Figure 2 shows the input and output connections. To reduce EMI noise, adding a ferrite core at the input and output cable is recommended.

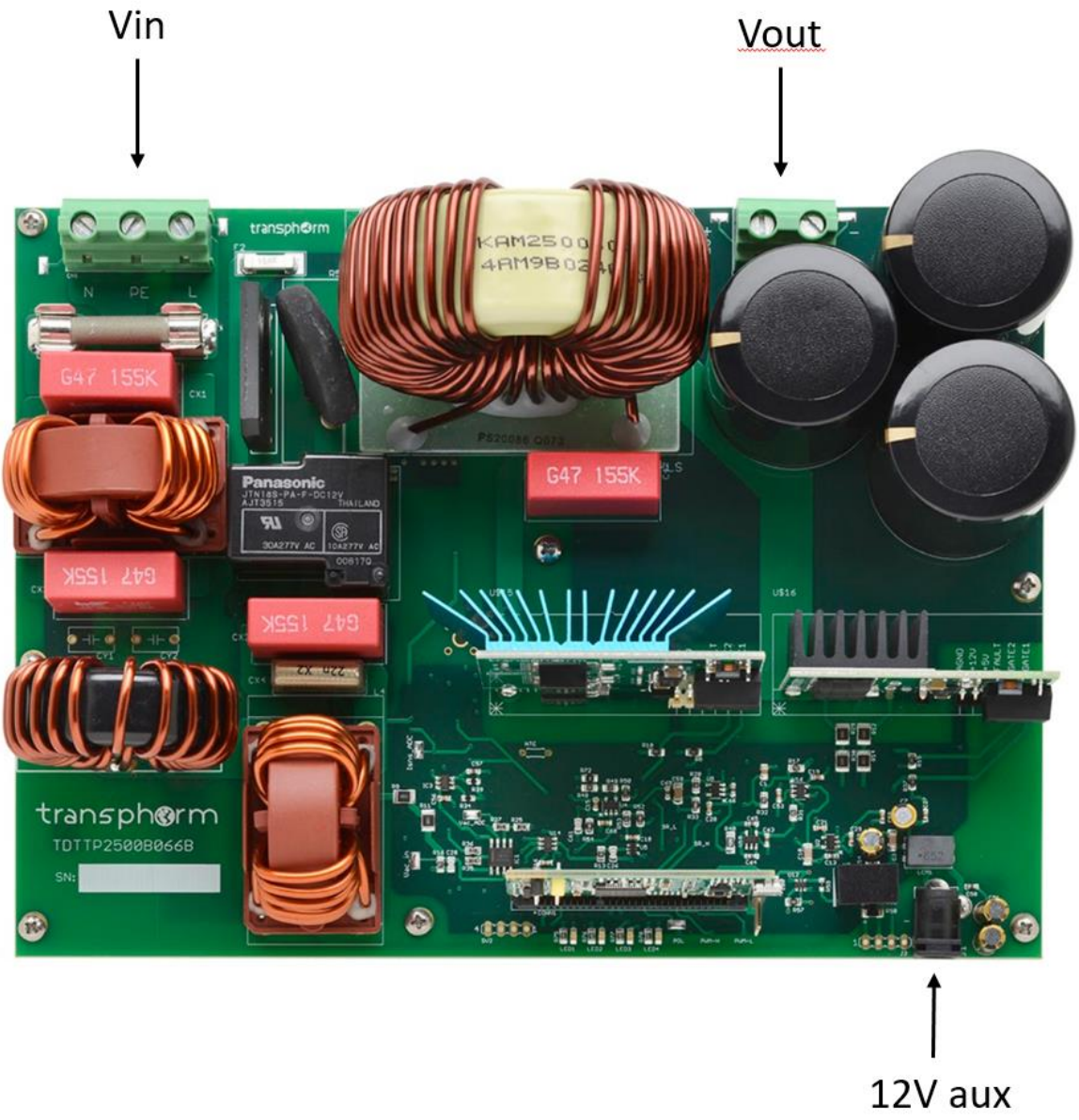


Figure 2. Input and output cable connections

Circuit description for Bridge-Less Totem-Pole PFC based on GaN FET

The Bridge-less totem-pole topology is shown in Fig 3 below. As shown in Fig 3(a), two GaN FETs and two diodes are used for the line rectification, while in Fig 3(b), the circuit is modified and the diodes are replaced by two low resistance silicon MOSFETs to eliminate diode drops and improve the efficiency. Further information and discussion on the performance and the characteristics of Bridge-less PFC circuit is provided in [1].

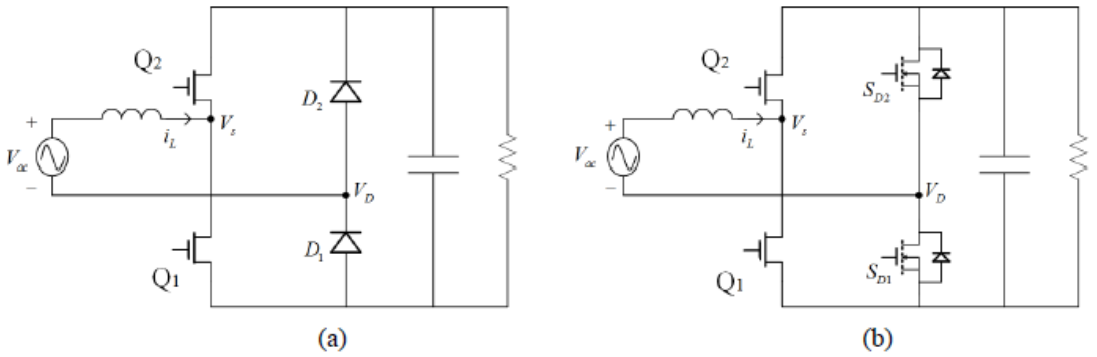


Fig.3 Totem-pole bridgeless PFC boost converter based on GaN FET (a) Diode for line rectification (b) MOSFET for line rectification

The large recovery charge (Qrr) of existing silicon MOSFETs makes CCM operation of a silicone totem-pole Bridge-less PFC impractical and reduces the total efficiency.

Figure 4(a) is a simplified schematic of a totem-pole PFC in continuous conduction mode (CCM) mode, focused on minimizing conduction losses. It comprises two fast-switching GaN FETs (Q1 and Q2) operating at a high pulse-width-modulation (PWM) frequency and two very low-resistance MOSFETs (S1 and S2) operating at a much slower line frequency (50Hz/60Hz). The primary current path includes one fast switch and one slow switch only, with no diode drop. The function of S1 and S2 is that of a synchronized rectifier as illustrated in Figures 4(b) and 4(c). During the positive AC cycle, S1 is on and S2 is off, forcing the AC neutral line tied to the negative terminal to the DC output. The opposite applies for the negative cycle.

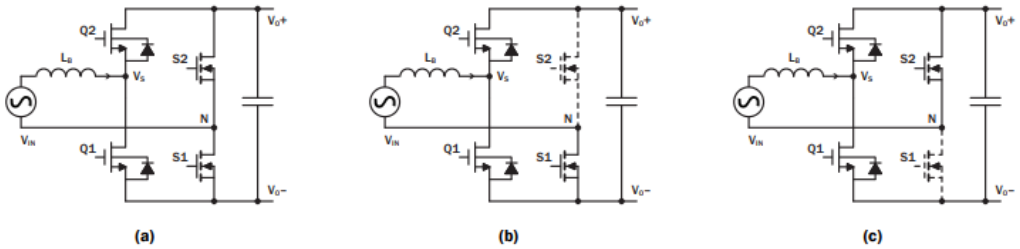


Figure 4. Totem-pole PFC with GaN FETs (a) simplified schematic, (b) during positive AC cycle and (c) during negative AC cycle

In either AC polarity, the two GaN FETs form a synchronized boost converter with one transistor acting as a master switch to allow energy intake by the boost inductor (LB), and another transistor as a slave switch to release energy to the DC output. The roles of the two GaN devices interchange when the polarity of the AC input changes; therefore, each transistor must be able to perform both master and slave functions. To avoid shoot-through a dead time is built in between two switching events, during which both transistors are momentarily off. To allow CCM operation, the body diode of the slave transistor must function as a flyback diode for the inductor current to flow during dead time. The diode current; however, must quickly reduce to zero and transition to the reverse blocking state once the master switch turns on. This is the critical process for a totem-pole PFC which, with the high Qrr of the body diode of high-voltage Si MOSFETs, results in abnormal spikes, instability, and associated high switching losses. The low Qrr of the GaN switches allows designers to overcome this barrier.

As seen in Figure 5, inductive tests at 430V bus show healthy voltage waveforms up to inductor current exceeding 35A using either a high-side (Figure 5(a)) or low-side (Figure 5(b)) GaN transistor as a master switch. With a design goal of 2.5kW output power in CCM mode at 230VAC input, the required inductor current is 20A. This test confirms a successful totem-pole power block with enough current overhead.

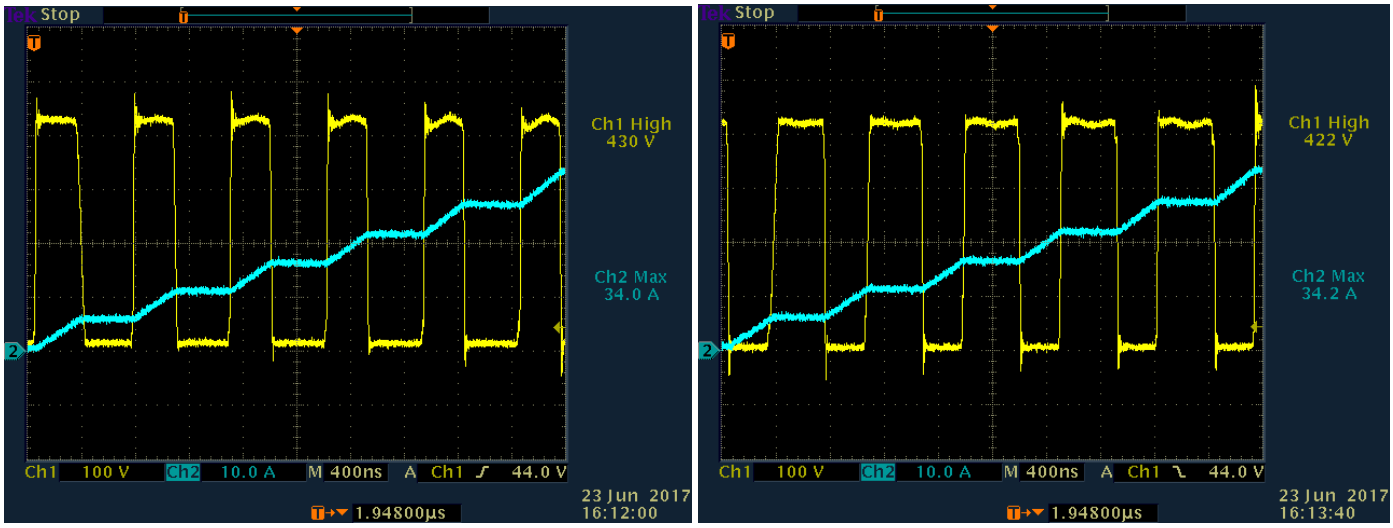


Fig 5. Hard-switched waveforms of a pair of GaN FET switches when setting a) high side as master and b) low side as master

One issue inherent in the bridgeless totem-pole PFC is the operation mode transition at AC voltage zero-crossing. For instance, when the circuit operation mode changes from positive half-line to negative half-line at the zero-crossing, the duty ratio of the high-side GaN switch changes abruptly from almost 100% to 0% and the duty ratio of low-side GaN switch changes from 0% to 100%. Due to the slow reverse recovery of diodes (or body diode of a MOSFET), the voltage VD cannot jump from ground to VDC instantly; a current spike will be induced. To avoid the problem, a soft-start at every zero-crossing is implemented to gently reverse duty ratio (a soft-start time of a few switching cycles is enough). The TDTTP2500B066B evaluation board is designed to run in CCM and the larger inductance alleviates the current spike issue at zero-crossing.

Dead time control

The required form of the gate-drive signals is shown in Figure 5. The times marked A are the dead times when neither transistor is driven on. The dead time must be greater than zero to avoid shoot-through currents. The Si8230 gate drive chip ensures a minimum dead time based on the value of resistor R24, connected to the DT input. The dead time in ns is equal to the resistance in kΩ x 10, so the default value of 20k corresponds to 200ns. This will add to any dead time already present in the input signals. The on-board pulse generator circuit; for example, creates dead times of about 60ns (see Figure 6). The resulting dead time at the gate pins of Q1 and Q2 is about 120ns. Either shorting or removing R7 will reduce the dead time to 60ns.

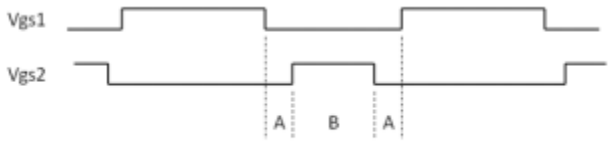


Figure 6. Non-overlapping gate pulses

While a typical Si MOSFET has a maximum dV/dt rating of 50V/ns, the TP65H050G4BS GaN FET will switch at dV/dt of 100V/ns or higher to achieve the lowest possible switching loss. At this level of operation, even the layout becomes a significant contributor to performance. As shown in Figure 8, the recommended layout keeps a minimum gate drive loop and keeps the traces between the switching nodes very short--with the shortest practical return trace to the power bus and ground. The power ground plane provides a large cross-sectional area to achieve an even ground potential throughout the circuit. The layout carefully separates the power ground and the IC (small signal) ground, only joining them at the source pin of the FET to avoid any possible ground loop. Note that the Transphorm GaN FETs in TO-263 packages have pinout configuration of G-S-D. The G-S-D configuration is designed with thorough consideration to minimize the gate source driving loop, reducing parasitic inductance and to separate the driving loop (gate source) and power loop (drain source) to minimize noise. All PCB layers of the TDTTP2500B066B design are shown Figure 8(a-c) and available in the design files.

Design details

A detailed circuit schematic of the TDTTP2500B066B Mother Board is shown in Figures 7 and 8, the PCB layers in Figure 9, and the parts list in Table 1 (also included in the design files).

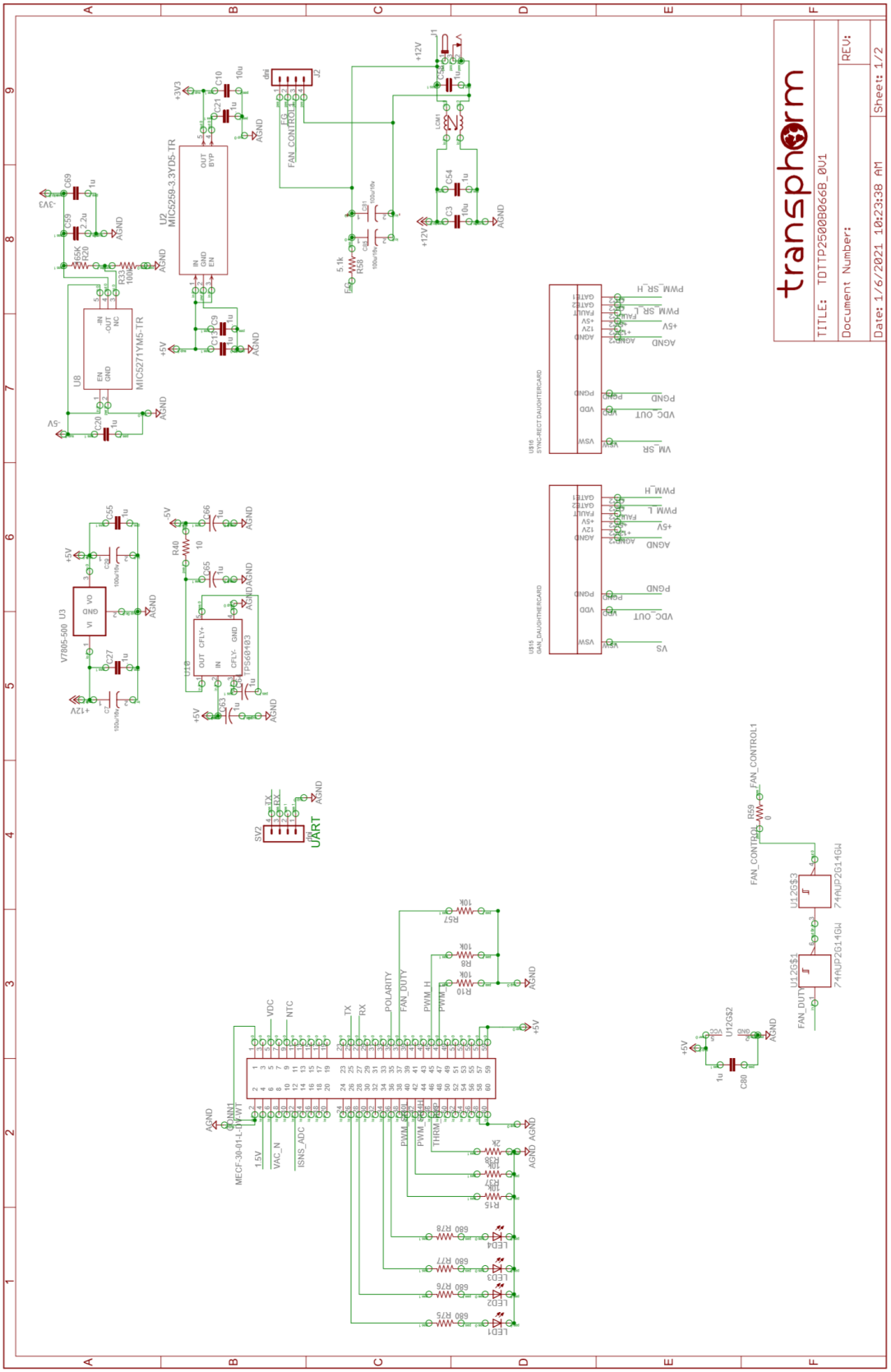


Fig 7

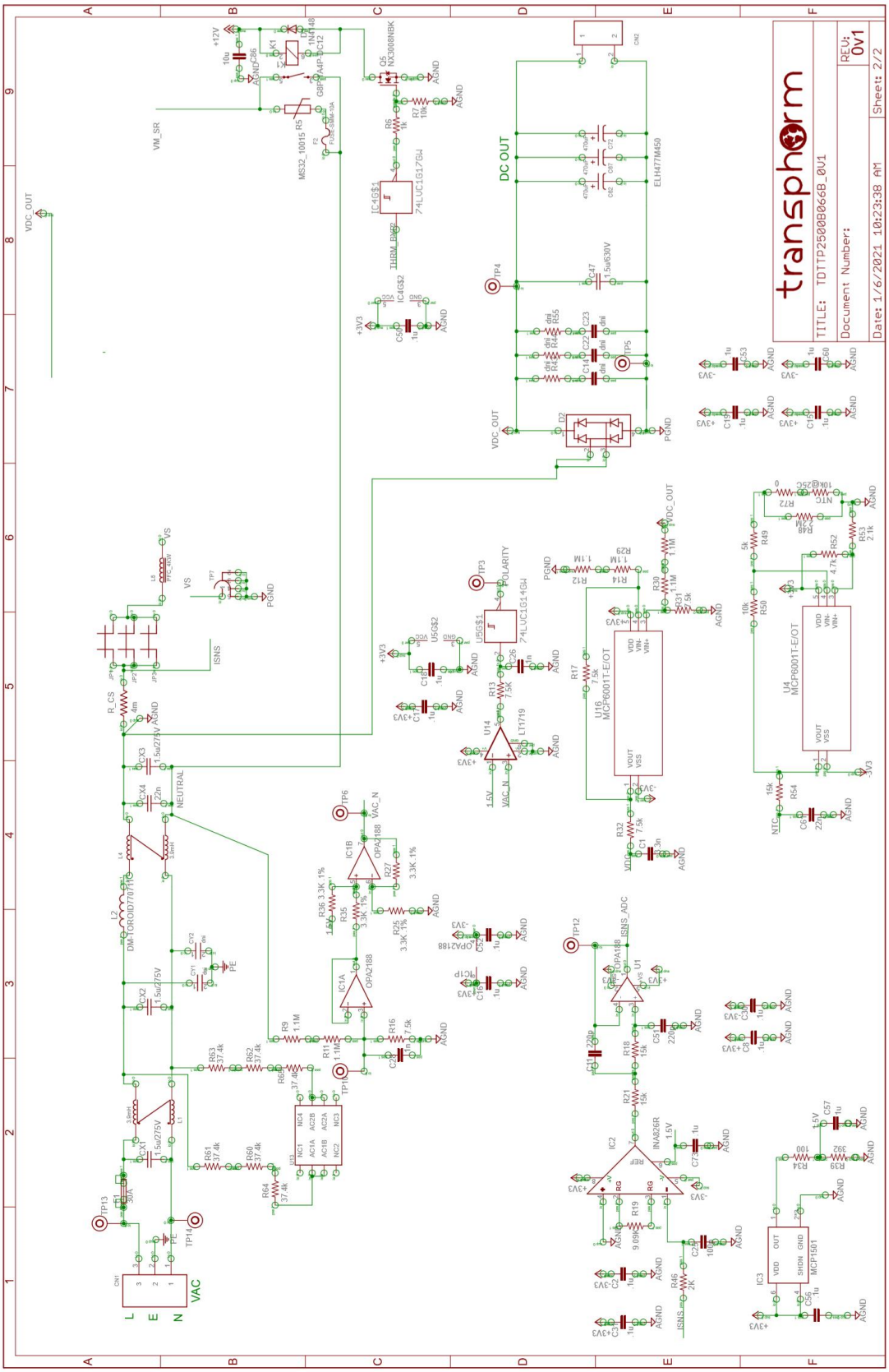


Fig 8

Table 1. TDTTP2500B066B evaluation board bill of materials (BOM)

Qty	Value	Device	Parts	Manufacturer PN
1		GBJ2506	D2	GBJ2506-BP
4		LEDCHIP-LED0805	LED1, LED2, LED3, LED4	SML-211UTT86
1		PJ-002AH	J1	PJ-002AH
8	dni	TESTPOINT-KEYSTONE5015	TP3, TP4, TP5, TP6, TP10, TP12, TP13, TP14	dni
21	.1u	C-EUC0603	C2, C8, C9, C15, C16, C17, C18, C19, C20, C21, C27, C30, C31, C50, C52, C53, C54, C55, C56, C60, C73	C0603C104J3RACTU
1	0	R-US_R0603	R59	RCS06030000Z0EA
1	0	R-US_R0805	R72	RC0805JR-070RL
6	1.1M	R-US_R1210	R9, R11, R12, R14, R29, R30	KTR25JZPF1104
3	1.5u/275V	ECQ-U2A474ML1.0U	CX1, CX2, CX3	890334026030cs
1	1.5u/630V	ECQ-U2A474ML1.0U	C47	890334026030cs
1	1N4148	DIODE-SOD123	D1	1N4148W-E3-18
1	1k	R-US_R0805	R6	ERJ-6ENF1001V
2	1n	C-EUC0805	C26, C28	CC0805KRX7R9BB102
5	1u	C-EUC0603	C13, C57, C58, C69, C80	TMK107B7105KA-T
4	1u	C-USC0603	C63, C64, C65, C66	TMK107B7105KA-T
1	2.1k	R-US_R0805	R53	RC0805FR-072K1L

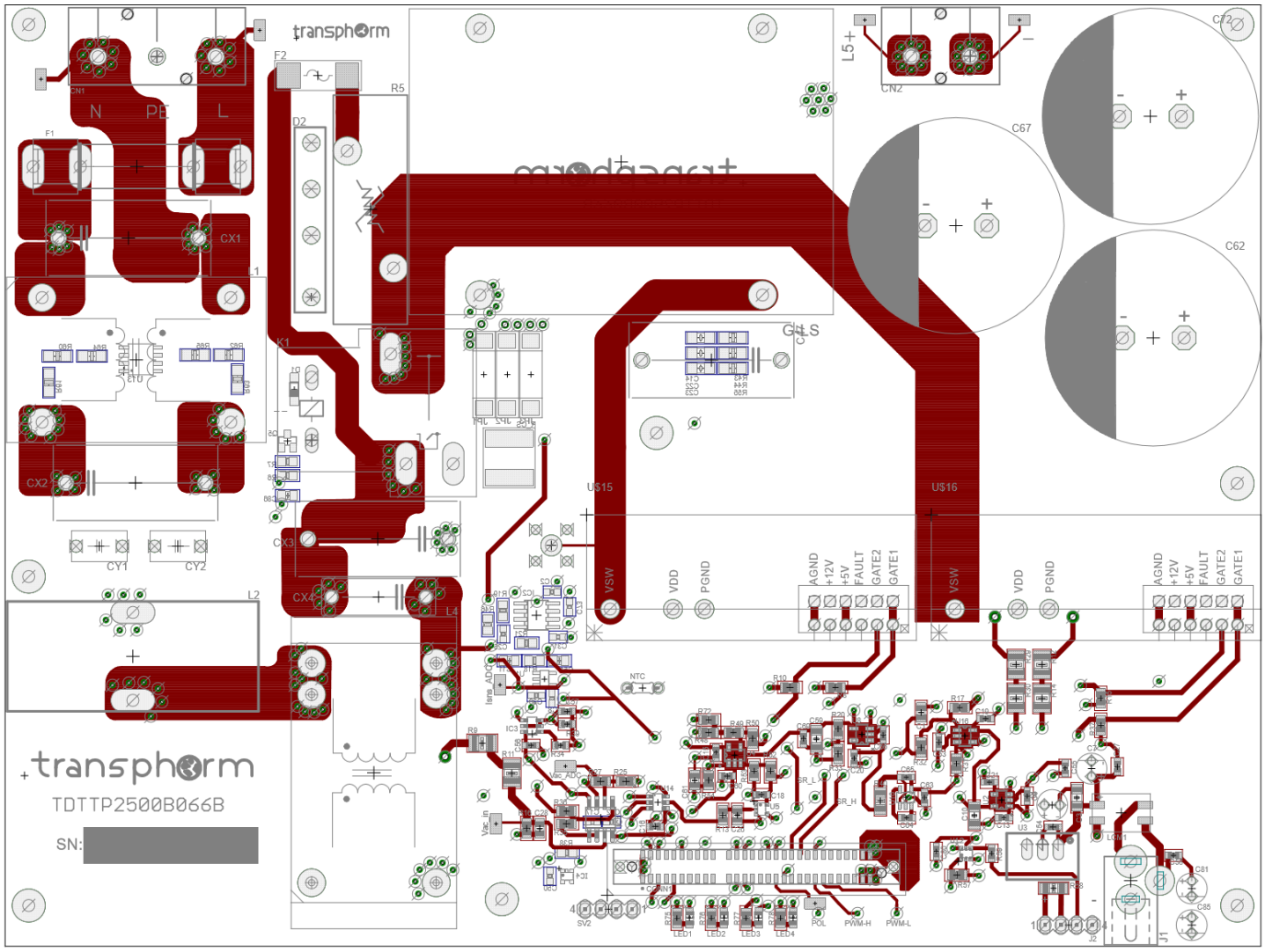
1	2.2M	R-US_R0805	R48	RMCF0805JT2M20
1	2.2u	C-EUC1206	C59	CL31B225KAHNNNE
1	2K	R-US_R0805	R46	ERJ-6ENF2001V
1	2PIN_9.53MM	2PIN_9.53MM	CN2	1714971
1	2k	R-US_R0805	R38	ERJ-6ENF2001V
4	3.3K .1%	R-US_R0805	R25, R27, R35, R36	ERA-6AEB332V
1	3.3n	C-EUC0805	C1	C0805C332K5RACTU
1	3.9mH	CMC_42X27MM_SM	L1	T60405-R6128-X225
1	3.9mH	CM_42X27MM_JC	L4	T60405-R6128-X225
1	3PIN_9.53MM	3PIN_9.53MM	CN1	1714984
1	4.7k	R-US_R0805	R52	RC0805FR-074K7L
1	4m	RES_CSSH2728	R_CS	CSSH2728FT4L00
1	5.1k	R-US_R1206	R58	RC1206FR-075K1L
1	5k	R-US_R0805	R49	RC0805FR-075K1L
1	7.5K	R-US_R0805	R13	ERJ-6ENF7501V
4	7.5k	R-US_R0805	R16, R17, R31, R32	RN73C2A7K5BTDF
1	9.09K	R-US_R0805	R19	ERJ-6ENF9091V
1	10	R-US_R1206	R40	ERJ-8ENF10R0V
3	dni	R-US_R1206	R43, R44, R55	dni
7	10k	R-US_R0805	R7, R8, R10, R15, R37, R50, R57	ERJ-6ENF1002V
1	dni	R-US_0204/5	NTC	dni
3	dni	C-EUC1206	C14, C22, C23	dni
1	10u	C-EUC0805	C86	GRM21BR61E106KA73L

2	10u	C-EUC1206	C3, C10	12063D106KAT2A
3	15k	R-US_R0805	R18, R21, R54	RC0805FR-0715KL
1	22n	C-EUC0805	C61	C2012C0G1V223J060AC
1	22n	ECQ-U2A474ML22N	CX4	PME271M522MR30
1	30A	SH32	F1	01020078H
6	37.4k	R-US_R1206	R60, R61, R62, R63, R64, R65	RC1206FR-0737K4L
1	74AUP2G14GW	74AUP2G14GW	U12	NC7WZ14P6X
1	74LVC1G14GW	74LVC1G14GW	U5	NC7SZ14M5X
1	74LVC1G17GW	74LVC1G17GW	IC4	SN74LVC1G17DBVR
1	100	R-US_R0603	R34	RC0603FR-07100RL
1	100k	R-US_R0805	R33	ERJ-6ENF1003V
1	100p	C-EUC0603	C25	06035A101FAT2A
4	100u/16v	ELE_CAP_D5MM_P2MM	C7, C29, C81, C85	UKL1C101KPDANA
1	165K	R-US_R0805	R20	ERJ-6ENF1653V
2	220p	C-EUC0805	C11, C51	CC0805KRX7R9BB221
1	392	R-US_R0603	R39	RC0603FR-07392RL
3	470uF	ELE_CAP_D35MM_P10MM	C62, C67, C72	ALC10A471DF450
4	680	R-US_R0805	R75, R76, R77, R78	RC0805FR-07680RL
1	CAP200DG	NCP4810	U13	CAP200DG
1	CMC_WURTH_744229	CMC_WURTH_744229	LCM1	744229
1	DM-TOROID770711	DM-TOROID770711	L2	CWS-1SN-12606
1	FUSE-SMM-10A	FUSE-SMM	F2	0463015.ER
1	G8P-1A4P-DC12	G8P-1A4P	K1	JTN1AS-PA-F-DC12V

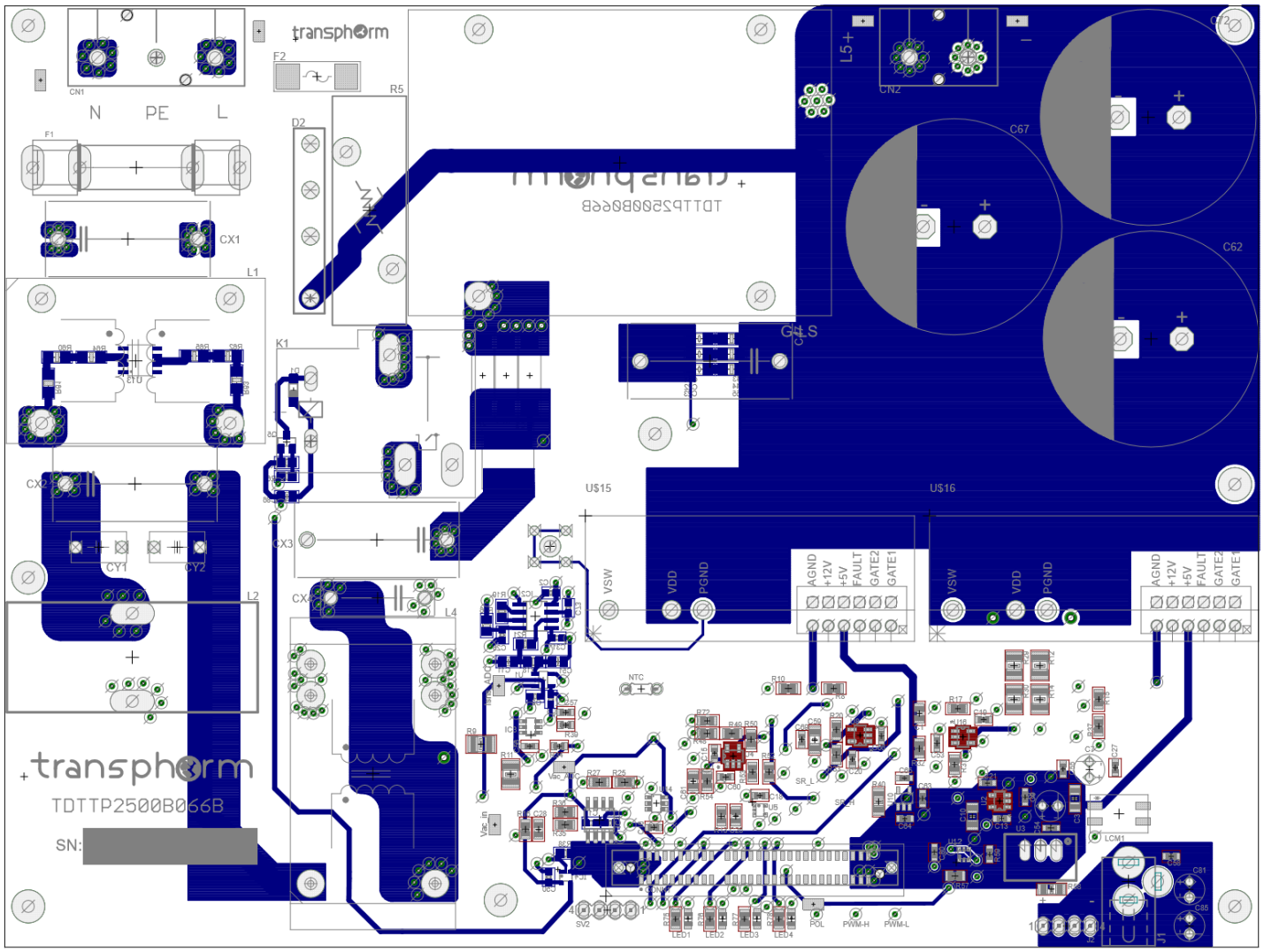
1	GAN_DAUGHTHER CARD	GAN_CARD_CONNECTOR_V2	U$15	see yellow highlighted section below.
1	INA826R	INA826R	IC2	INA826AID
3	JUMPER_S1621-46R	JUMPER_S1621-46R	JP1, JP2, JP3	S1621-46R
1	LT1719	LT1719	U14	LT1719CS6#TRMPBF
1	MCP1501T-18E/CHY	MCP1501T-18E/CHY	IC3	MCP1501T-18E/CHY
2	MCP6001T-E/OT	MCP6001T-E/OT	U4, U16	MCP6001T-E/OT
1	MECF-30-01-L-DV-WT	MECF-30-01-L-DV-WT	CONN1	MECF-30-01-L-DV-WT
1	MIC5259-3.3YD5-TR	MIC5259-3.3YD5-TR	U2	MIC5259-3.3YD5-TR
1	MIC5271YM5-TR	MIC5271YM5-TR	U8	MIC5271YM5-TR
1	MS32_10015	MS35_10018	R5	MS32 10015-B
1	NX3008NBK	BSS138-7-F	Q5	NX3008NBK,215
1	OPA188	AD8031RJ	U1	OPA188AIDBVT
1	OPA2188	AD826R	IC1	OPA2188AIDR
1	PFC_4KW	PFC_4KW	L5	T91880B
1	SYNC-RECT DAUGHTERCARD	GAN_CARD_CONNECTOR_V2	U$16	see yellow highlighted section below.
1	TPS60403	TPS60403	U10	TPS60403DBVR
1	V7805-500	V7805-500	U3	TR05S05
2	dni	MA04-1	J2, SV2	dni
1	dni	TEKTRONIX-PCB	TP7	dni
2	dni	VY2_CAP_SAFETY	CY1, CY2	dni
8	stand off (nylon 1/2)	stand off (nylon 1/2)	stand off (nylon 1/2)	1902C
8	machine screw (ss 1/2)	machine screw (ss 1/2)	machine screw (ss 1/2)	9902

6	U$15, U$16 part 1	GAN_DAUGHTERCARD and SYNC-RECT DAUGHTERCARD	PGND, VDD, VSW	a32386-nd
2	U$15, U$16 part 2	GAN_DAUGHTERCARD and SYNC-RECT DAUGHTERCARD	U$15, U$16	WM18605-ND

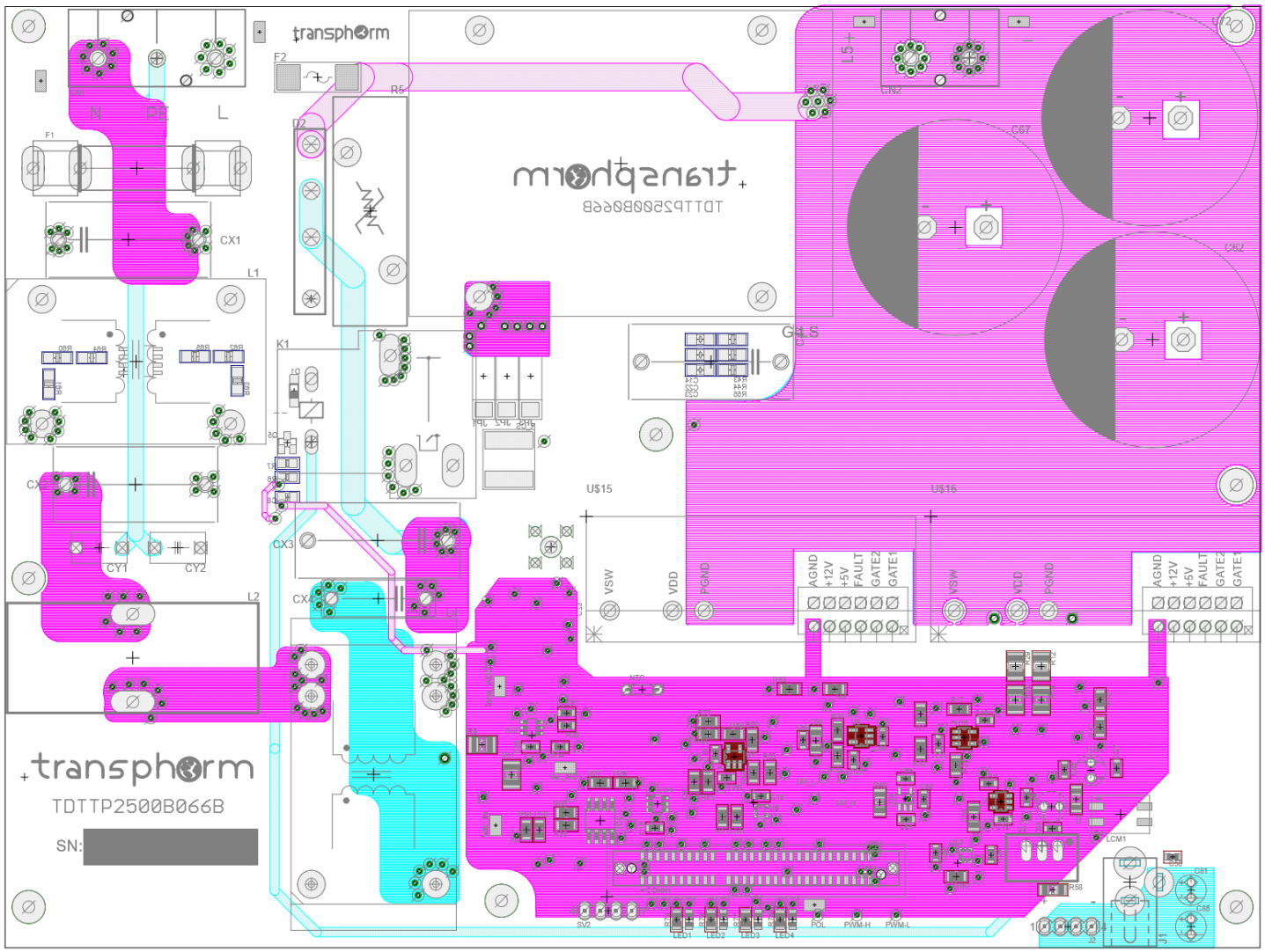
For this evaluation board, the PFC circuit has been implemented on a 4-layer PCB. The GaN FET half-bridge is built with TP65H050G4BS (0.050 ohm) devices by Transphorm, Inc. The slow Si switches are IPT65R033G7XTMA1 super junction MOSFETs with 0.033 ohm on-resistance. The inductor is made of a High Flux core with the inductance of 480 uH and a dc resistance of 0.025 Ohm, designed to operate at 66 kHz. A simple 0.5 A rated high/low side driver IC (Si8230) with 0/12 V as on/off states directly drives each GaN FETs. A dsPIC33CK256MP506 Digital Power PIM MA330048 handles the control algorithm. The voltage and current loop controls are similar to conventional boost PFC converter. The feedback signals are dc output voltage (VO), ac input potentials (V_{ACP} and V_{ACN}) and inductor current (I_L). The input voltage polarity and RMS value are determined from V_{ACP} and V_{ACN}. The outer voltage loop output multiplied by $|V_{AC}|$ gives a sinusoidal current reference. The current loop gives the proper duty ratio for the boost circuit. The polarity determines how PWM signal is distributed to drive Q1 and Q2. A soft-start sequence with a duty ratio ramp is employed for a short period at each ac zero-crossing for better stability.



(a) PCB top layer



(b) PCB bottom layer



(c) PCB inner layer 2 (ground plane) + inner layer 3 (power plane)

Figure 9. TDTTP2500B066B Mother Board PCB layers

Using the board

The mother board can be used for evaluation of Transphorm GaN 0.050 ohm TP65H050G4BS FETs, mounted on the **TDHB-65H050G4BS-DC** in a Bridge-less totem-pole PFC circuit.

It is not a complete circuit, but rather a building block.

Mother board Setup:

1. Connect programmed microchip PIM onto CONN1
2. Place **TDHB-65H050G4BS-DC** GaN Daughter card and **Sync-Rect** Daughter card onto TDTTP2500B066B main board (U$15 and U$16 locations). The design files for the daughtecard are available at Transphormusa.com

Figure 10. TDHB-65H050G4BS-DC

Figure 11. Sync-Rect Daughtercard

Turn on Sequences:

1) Connect an Electronic / resistive load to the corresponding marking (CN2).

The requirement for the resistive load:

– At 115 Vac input: 350 W and ≤ 1250 W

– At 230 Vac input: 350 W and ≤ 2500 W

2) Connect the 12 Vdc auxiliary supply to the demo-board (included in the demo-kit package).

- Verify auxiliary LED is on.

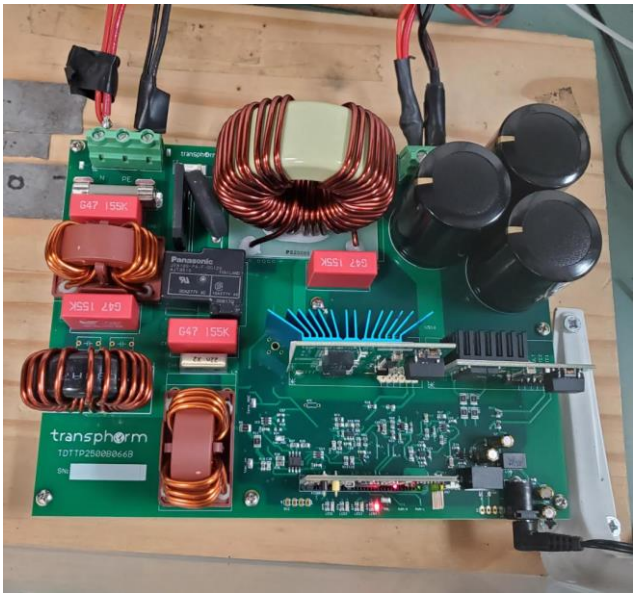


Figure 12. Test setup

3) With HV power off, connect the high-voltage AC power input to the corresponding marking (CN1) on the PCB;

-N and L (PE: potential ground)

4) Turn on the AC power input (85 Vac to 265 Vac; 50 – 60Hz)

a. Minimum power load for turn-on sequence is 350W.

Monitor CN2 output voltage with Vdc meter to verify 385V +/- 5V is generated.

b. Electronic / resistive load can be increased while AC supply is ON and board is functional.

Turn off sequences:

1) Switch off the high-voltage AC power input;

2) Power off dc bias.

3) Verify Input and Output voltage = 0.

Efficiency Sweep and EMI

For the efficiency measurement, the input/output voltage and current will be measured for the input/output power calculation with a power analyzer. Efficiency has been measured at 120 Vac or 230 Vac input and 400 Vdc output using the WT1800 precision power analyzer from Yokogawa. The efficiency results for this Totem Pole PFC board are shown in Fig.16. The extremely high efficiency of 99% at 230Vac input, and > 98% at 120V ac input is the highest among PFC designs with similar PWM frequency; this high efficiency will enable customers to reach peak system efficiency to meet and exceed Titanium standards.

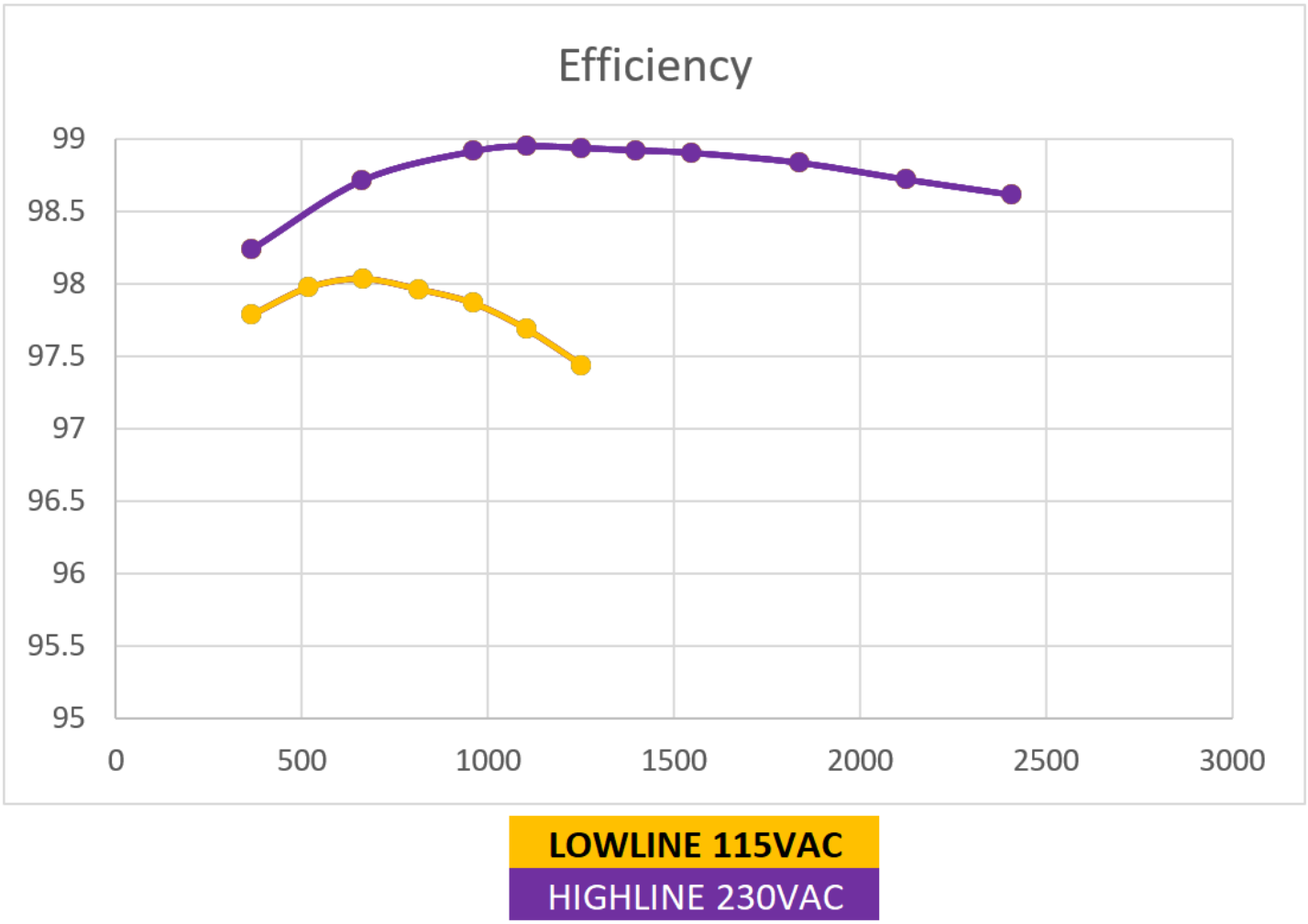


Figure 16. The efficiency results for Bridge-less Totem-pole PFC Evaluation Board.

The THDi is measured using WT1800 at the condition of input THDv 3.8%. As shown in Fig 17 below, it meets the standard of IEC61000-3-12.

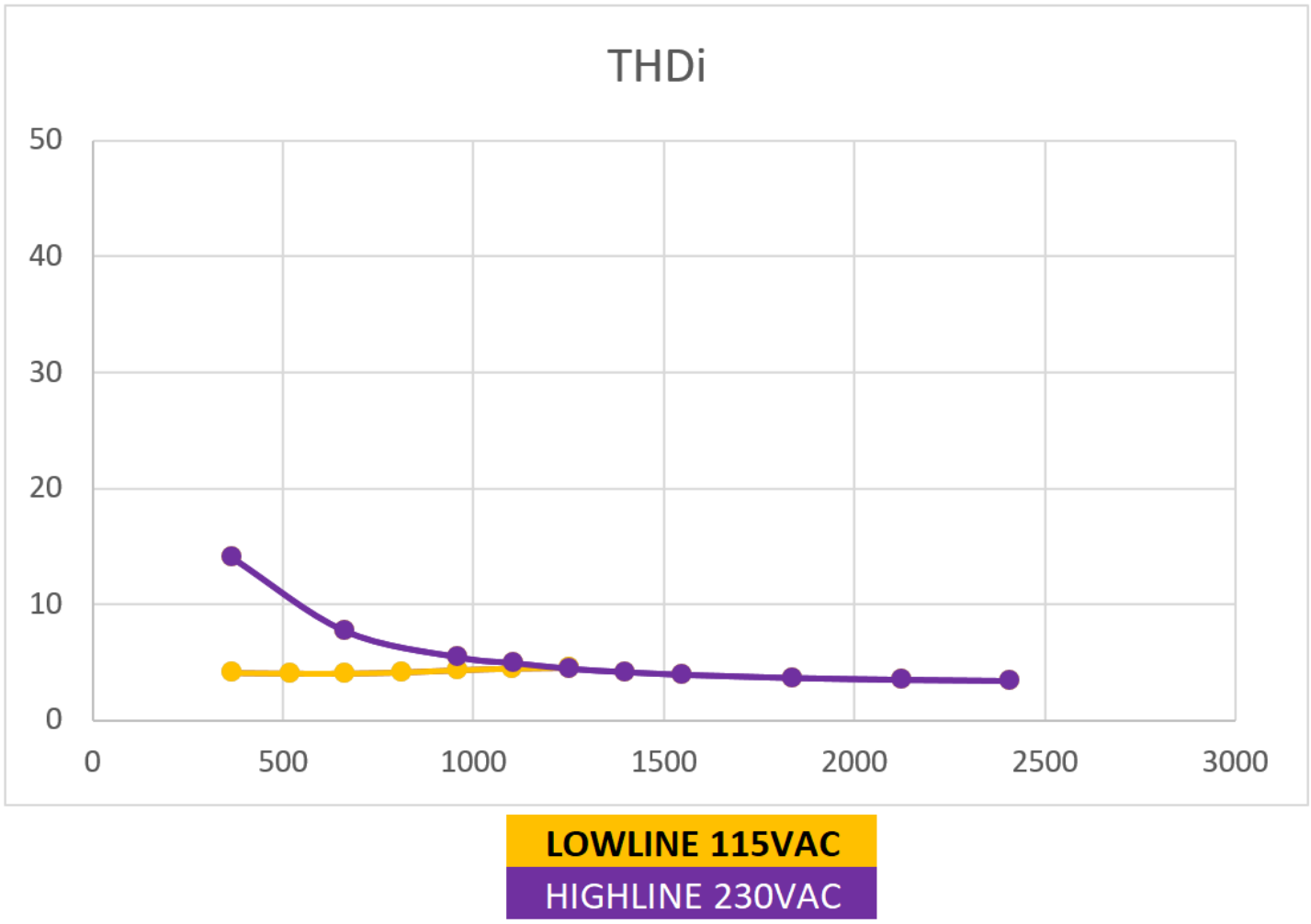


Fig 17. THDi meets IEC61000-3-12

Maximum Load Limit:

The TDTTP2500B066B Bridge-less totem-pole PFC eval board is allowed to run overload in a short time. The rated input current for < 230Vac input is 18A, and the 10% overload current can be 11A. The input OCP will be triggered when the current is over 12A.

WARNINGS:

This demo board is intended to demonstrate GaN FET technology. While it provides the main features of a totem-pole PFC, it is not intended to be a finished product and does not have all the protection features found in commercial power supplies. Along with this explanation go a few warnings which should be kept in mind:

1. An isolated AC source should be used as input; an isolated lab bench grade power supply or the included AUX DC supply should also be used for the 12V DC power supply. Float the oscilloscope by using an isolated oscilloscope or by disabling the PE (Protective Earth) pin in the power plug. Float the current probe power supply (if any) by disabling the PE pin in the power plug.

2. Use a resistive load only. The Totem-pole PFC kit can work at zero load with burst mode. The output voltage will be swinging between 375V and 385V during burst mode.

3. The demo board is not fully tested at large load steps. DO NOT apply a very large step in the load (>1000W) when it is running.

4. DO NOT manually probe the waveforms when the demo is running. Set up probing before powering up the demo board.

5. The auxiliary Vdc supply must be 12 V. The demo board will not work under, for example, 10 V or over 15V Vdc.

6. DO NOT touch any part of the demo board when it is running.

7. When plugging the control cards into the socket, make sure the control cards are fully pushed down with a clicking sound.

8. If the demo circuit goes into protection mode it will work as a diode bridge by shutting down all PWM functions. Recycle the bias power supply to reset the DSP and exit protection mode.

9. DO NOT use a passive probe to measure control circuit signals and power circuit signals in the same time. GND1 and AGND are not the same ground.

10. To get clean Vgs of low side GaN FET, it is recommended not to measure the Vds at the same time.

11. It is not recommended using passive voltage probe for Vds, Vgs measurement and using differential voltage probe for Vin measure measurement at the same time unless the differential probe has very good dv/dt immunity.

REFERENCE:

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