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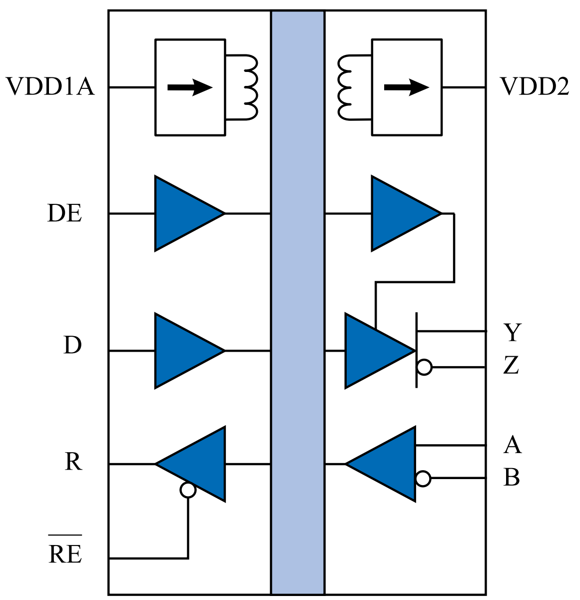
NVE CORPORATION

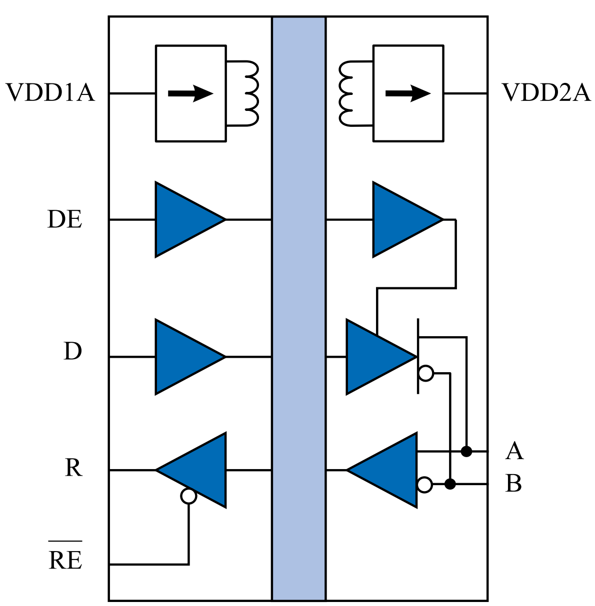
# IL4622E / IL4685E

# High-Speed Isolated 3.3 V Bus RS-422 / RS-485 Transceivers with Integrated DC-DC Convertors

## Block Diagrams




**IL4622**




**IL4685**

## Features

- 40 Mbps transceiver
- Integrated ¼ watt, 3.3-to-3.3 V DC-DC convertor
- 3.3 V bus
- 1/5 Unit Load; 160 node fanout
- 2500 $V_{RMS}$ isolation voltage
- Up to 16.5 kV bus ESD protection
- Full failsafe
- Overcurrent protection
- Thermal shutdown protection
- –40 °C to 85 °C temperature range
- Low EMI without ferrite beads
- UL1577 listed; VDE V 0884-11 pending
- 0.3" True 8™ mm 16-pin SOIC package

## Applications

- Transportation systems
- Factory automation
- Industrial control networks
- Building environmental controls

## Description

The IL4622E and IL4685E are high-speed, fully-isolated, differential bus transceivers with integrated 3.3-to-3.3 V, one-quarter watt DC-DC convertors to provide a fully-isolated 3.3 V bus supply using the controller (UART) supply. This level of integration dramatically reduces chip count and board area.

The IL4622E has full-duplex connections for RS-422 busses; the IL4685E has a half-duplex transceiver generally used with RS-485.

The devices use NVE's proven, patented* spintronic Giant Magnetoresistance (GMR) isolation technology and IsoLoop® high-efficiency micro-scale isolation transformers.

A unique ceramic/polymer composite barrier provides full isolation and virtually unlimited barrier life.

Frequency hopping and shielding minimize EMI.

Current limiting and thermal shutdown features protect against bus short circuits and contention that may cause excessive power dissipation.

IsoLoop® is a registered trademark of NVE Corporation.
*U.S. Patent number 5,831,426; 6,300,617 and others.

**Rev. A**

## Truth Tables

### IL4622E Receiver

| $\overline{RE}$ | R | $V_{(A-B)}$ |
|---|---|---|
| H | Z | X |
| L | H | ≥ 200 mV |
| L | L | ≤–200 mV |
| L | H | Open |

### IL4622E Driver

| DE | D | $V_{(Y-Z)}$ |
|---|---|---|
| L | X | Z |
| H | H | ≥ 200 mV |
| H | L | ≤–200 mV |

### IL4685E

| $V_{ID}$ (A-B) | DE | $\overline{RE}$ | R | D | Mode |
|---|---|---|---|---|---|
| ≥ 200 mV | L | L | H | X | Receive |
| ≤–200 mV | L | L | L | X | Receive |
| ≥ 1.5 V | H | L | H | H | Drive |
| ≤–1.5 V | H | L | L | L | Drive |
| X | X | H | Z | X | Hi-Z R |
| Open | L | L | H | X | Receive |



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### Absolute Maximum Ratings[(1)]

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Storage temperature | $T_S$ | –55 | | 150 | °C | |
| Junction temperature | $T_J$ | –55 | | 150 | °C | |
| Voltage range at A or B bus pins | | –7 | | 12 | V | |
| Supply voltage | $V_{DD1A}$, $V_{DD1B}$, $V_{DD2A}$, $V_{DD2B}$ | –0.5 | | 6 | V | |
| Digital input voltage | | –0.5 | | $V_{DD}$ + 0.5 | V | |
| Digital output voltage | | –0.5 | | $V_{DD}$ + 1 | V | |
| ESD (bus nodes) | | | | | | |
| IL4685 or IL4622 configured as half-duplex | | ±16.5 | | | kV | IEC61000-4-2 |
| IL4622 configured as full-duplex | | ±12 | | | kV | IEC61000-4-2 |
| EFT (bus nodes) | | 4 | | | kV | IEC61000-4-4 Level 4 |

### Recommended Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| DC-DC convertor input voltage | $V_{DD1A}$ | 3 | 3.3 | 3.6 | V | |
| Transceiver controller-side supply | $V_{DD1B}$ | 3 | 3.3 | 5.5 | V | |
| Transceiver bus-side supply voltage | $V_{DD2B}$ | 3 | 3.3 | 3.5 | V | |
| Ambient operating temperature | $T_{min}$; $T_{max}$ | –40 | | 85 | °C | |
| Junction temperature | $T_J$ | –40 | | 140 | °C | |
| High-level digital input voltage | $V_{IH}$ | 2.4 | | $V_{DD1}$ | V | $V_{DD1}$ = 3.3 V |
| Low-level digital input voltage | $V_{IL}$ | 0 | | 0.8 | V | |
| Differential input voltage[(2)] | $V_{ID}$ | | | +12 / –7 | V | |
| High-level output current (driver) | $I_{OH}$ | | | 60 | mA | |
| High-level digital output current (receiver) | $I_{OH}$ | | | 8 | mA | |
| Low-level output current (driver) | $I_{OL}$ | –60 | | | mA | |
| Low-level digital output current (receiver) | $I_{OL}$ | –8 | | | mA | |
| Digital input signal rise and fall times | $t_{IR}$, $t_{IF}$ | DC Stable | | | | |

## Safety and Approvals

***VDE V 0884-11 / IEC 60747-17*** (Basic Isolation; pending under VDE File Number 5016933-4880-0001)

- Isolation voltage ($V_{ISO}$): 2500 $V_{RMS}$
- Transient overvoltage ($V_{IOTM}$): 4000 $V_{PK}$
- Surge rating: 4000 V
- Each part tested at 1590 $V_{PK}$ for 1 second, 5 pC partial discharge limit.
- Samples tested at 4000 $V_{PK}$ for 60 sec.; then 1358 $V_{PK}$ for 10 sec. with 5 pC partial discharge limit.
- Working Voltage ($V_{IORM}$; pollution degree 2): 1000 $V_{RMS}$

| Safety-Limiting Values | Symbol | Value | Units |
|---|---|---|---|
| Safety rating ambient temperature | $T_S$ | 180 | °C |
| Safety rating power (180 °C) | $P_S$ | 270 | mW |
| Supply current safety rating (total of supplies) | $I_S$ | 54 | mA |

***UL 1577*** (Component Recognition Program File Number E207481)

- 2500 V rating
- Each part tested at 3000 $V_{RMS}$ (4243 $V_{PK}$) for 1 second
- Each lot sample tested at 2500 $V_{RMS}$ (3536 $V_{PK}$) for 1 minute

## Soldering Profile

Per JEDEC J-STD-020C, MSL 1


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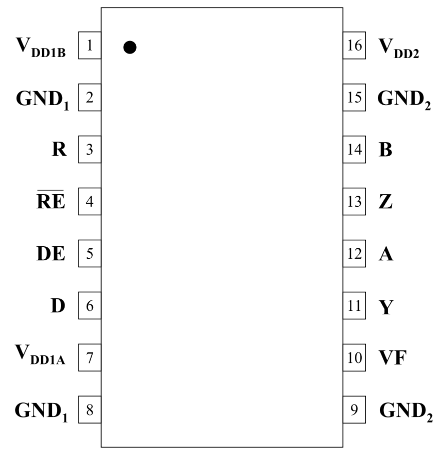
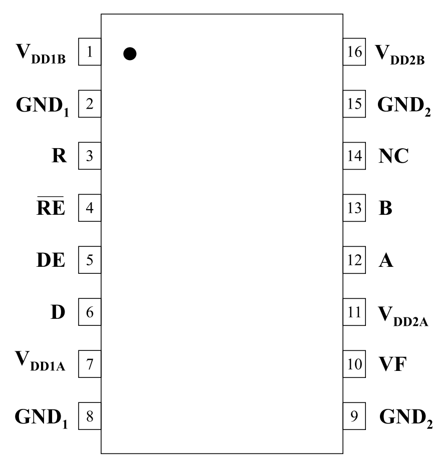
## IL4622E Pin Connections

| | | |
|---|---|---|
| 1 | VDD1B | Transceiver controller-side power supply input (3.3 V nominal). |
| 2 | $GND_1$ | Input power supply ground (pin 2 is internally connected to pin 8). |
| 3 | R | Output data from bus. |
| 4 | $\overline{RE}$ | Read data enable. If $\overline{RE}$ is high, R = high impedance; has a 500 kΩ nominal internal pulldown. |
| 5 | DE | Drive enable (has a 1 MΩ nominal internal pulldown). |
| 6 | D | Data input to bus. |
| 7 | VDD1A | DC-DC convertor input voltage (3.3 V nominal); bypass with 0.1 μF. |
| 8 | $GND_1$ | Input power supply ground (pin 8 is internally connected to pin 2). |
| 9 | $GND_2$ | Output power supply ground (pin 9 is internally connected to pin 15). |
| 10 | VF | Output-side rectifier output / regulator input; connect to a 0.1 μF/16 V external filter capacitor. |
| 11 | Y | Non-inverting bus driver. |
| 12 | A | Non-inverting bus receiver. |
| 13 | Z | Inverting bus driver. |
| 14 | B | Inverting bus receiver. |
| 15 | $GND_2$ | Output power supply ground (pin 15 is internally connected to pin 9). |
| 16 | VDD2 | DC-DC convertor output (3.3 V typical); internally powers transceiver functions. Bypass with 10 μF ceramic. |




## IL4685E Pin Connections

| | | |
|---|---|---|
| 1 | VDD1B | Transceiver controller-side power supply input (3.3 V nominal). |
| 2 | $GND_1$ | Input power supply ground (pin 2 is internally connected to pin 8). |
| 3 | R | Output data from bus. |
| 4 | $\overline{RE}$ | Read data enable (if $\overline{RE}$ is high, R = high impedance). |
| 5 | DE | Drive enable (has a 1 MΩ nominal internal pulldown). |
| 6 | D | Data input to bus. |
| 7 | VDD1A | DC-DC convertor input voltage (3.3 V nominal); bypass with 0.1 μF. |
| 8 | $GND_1$ | Input power supply ground (pin 8 is internally connected to pin 2). |
| 9 | $GND_2$ | Output power supply ground (pin 9 is internally connected to pin 15). |
| 10 | VF | Output-side rectifier output / regulator input; connect to a 0.1 μF/16 V external filter capacitor. |
| 11 | VDD2A | DC-DC convertor output (3.3 V typical) ); bypass with 10 μF ceramic. |
| 12 | A | Non-inverting bus line. |
| 13 | B | Inverting bus line. |
| 14 | NC | No internal connection. |
| 15 | $GND_2$ | Output power supply ground (pin 15 is internally connected to pin 9). |
| 16 | VDD2B | Transceiver power supply input<br>(connect to pin 11 to use DC-DC convertor). |



### Transceiver Bus Driver

| $T_{min}$ to $T_{max}$ and $V_{DD2B}$ = 3.1 V to 3.5 V unless otherwise stated | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.**(5) | **Max.** | **Units** | **Test Conditions** |
| Output voltage | $V_O$ | | | $V_{DD}$ | V | $I_O = 0$ |
| Differential output voltage | $\lvert V_{OD1}\rvert$ | | | $V_{DD}$ | V | $I_O = 0$ |
| Differential output voltage | $\lvert V_{OD2}\rvert$ | 2.1 | 3 | 3.5 | V | $R_L$ = 60 Ω |
| Differential output voltage | $\lvert V_{OD3}\rvert$ | 1.9 | | 3.5 | V | $R_L$ = 54 Ω |
| Change in magnitude of differential output voltage(3) | $\Delta\lvert V_{OD}\rvert$ | | | ±0.2 | V | $R_L$ = 54 Ω or 100 Ω |
| Common mode output voltage | $V_{OC}$ | | | 3 | V | $R_L$ = 54 Ω or 100 Ω |
| Change in magnitude of common mode output voltage(3) | $\Delta\lvert V_{OC}\rvert$ | | | ±0.2 | V | $R_L$ = 54 Ω or 100 Ω |
| High level input current | $I_{IH}$ | | | 10 | μA | $V_I$ = 3.5 V |
| Low level input current | $I_{IL}$ | | | −10 | μA | $V_I$ = 0.4 V |
| Absolute \|short-circuit output current\| | $I_{OS}$ | | | 250 | mA | $-7\text{ V} < V_O < 12\text{ V}$ |

### Transceiver Bus Receiver

| $T_{min}$ to $T_{max}$ and $V_{DD2B}$ = 3.1 V to 3.5 V unless otherwise stated | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.**(5) | **Max.** | **Units** | **Test Conditions** |
| Positive-going input threshold voltage | $V_{IT+}$ | | | 0.2 | V | $-7\text{ V} < V_{CM} < 12\text{ V}$ |
| Negative-going input threshold voltage | $V_{IT-}$ | −0.2 | | | V | $-7\text{ V} < V_{CM} < 12\text{ V}$ |
| Input hysteresis voltage | $(V_{IT+} - V_{IT-})$ | | 28 | | mV | $V_{CM}$ = 0 V, T = 25°C |
| Differential bus input capacitance | $C_D$ | | 9 | 12 | pF | |
| High-level output voltage | $V_{OH}$ | $V_{DD} - 0.2$ | $V_{DD}$ | | V | $V_{ID}$ = 200 mV<br>$I_{OH}$ = −20 μA |
| Low-level output voltage | $V_{OL}$ | | | 0.2 | V | $V_{ID}$ = −200 mV<br>$I_{OH}$ = 20 μA |
| High-impedance-state bus output current | $I_{OZ}$ | | | ±1 | μA | $V_O$ = 0.4 to ($V_{DD2}$−0.5) V |
| Bus line input current | $I_I$ | | | 220 | μA | $V_I$ = 12 V |
| | | | | −160 | μA | $V_I$ = −7 V |
| Bus line input resistance | $R_I$ | 60 | 80 | | kΩ | |

### Transceiver Switching Specifications

| $T_{min}$ to $T_{max}$; $V_{DD1B}$ = 3 V to 3.45 V; $V_{DD2B}$ = 3.1 V to 3.5 V | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.**(5) | **Max.** | **Units** | **Test Conditions** |
| Data rate | | 40 | | | Mbps | $R_L$ = 54 Ω, $C_L$ = 50 pF |
| Propagation delay(4) | $t_{PD}$ | | 25 | 35 | ns | $V_O$ = −1.5 to 1.5 V,<br>$C_L$ = 15 pF |
| Pulse skew(5) | $t_{SK}(P)$ | | 2 | 5 | ns | $V_O$ = −1.5 to 1.5 V,<br>$C_L$ = 15 pF |
| Skew limit(6) | $t_{SK}(LIM)$ | | 4 | 10 | ns | $R_L$ = 54 Ω, $C_L$ = 50 pF |
| Output enable time to high level | $t_{PZH}$ | | 17 | 30 | ns | $C_L$ = 15 pF |
| Output enable time to low level | $t_{PZL}$ | | 17 | 30 | ns | $C_L$ = 15 pF |
| Output disable time from high level | $t_{PHZ}$ | | 17 | 30 | ns | $C_L$ = 15 pF |
| Output Disable Time From Low Level | $t_{PLZ}$ | | 17 | 30 | ns | $C_L$ = 15 pF |
| Common mode transient immunity (output logic high to logic low) | $\lvert CM_H\rvert,\lvert CM_L\rvert$ | 30 | 50 | | kV/μs | $V_{CM}$ = 1500 $V_{DC}$<br>$t_{TRANSIENT}$ = 25 ns |

### Transceiver Section Power Consumption

| $T_{min}$ to $T_{max}$; $V_{DD1B}$ = 3 V to 3.45 V; $V_{DD1B}$ = 3.1 V to 3.5 V unless otherwise specified | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.**[5] | **Max.** | **Units** | **Test Conditions** |
| Controller-side Quiescent supply $V_{DD1B}$ = 3.3 V | $I_{DD1B}$ | | 1 | 2 | mA | No load ($R_T = \infty$); Outputs Enabled; $f_{IN}$ = 0 Hz |
| Controller-side Quiescent supply $V_{DD1B}$ = 5 V | $I_{DD1B}$ | | 1.7 | 4 | mA | |
| Bus-side quiescent supply current | $I_{DD2B}$ | | 4 | 6 | mA | |
| Controller-side dynamic supply current | $I_{DD1B}$ | | 0.18 | | mA/Mbps | |
| Bus-side dynamic supply current | $I_{DD2B}$ | | 0.75 | | mA/Mbps | $R_T = \infty$ |
| | | | 0.55 | | mA/Mbps | $R_T = 60\ \Omega$ |
| Transceiver power dissipation | $I_{DD1B} \times V_{DD1B} + I_{DD2B} \times V_{DD2B}$ | | 17 | | mW | $R_T = \infty$; $f_{IN}$ = 0 Hz |
| | | | 150 | | mW | $R_T$= 60Ω; $f_{IN}$=40 Mbps; excludes $R_T$ power dissipation |

### Transceiver Field Immunity[7]

| $V_{DD1B}$ = 3.3 V, $V_{DD2B}$ = 3.3 V | | | | | | |
|---|---|---|---|---|---|---|
| Power frequency magnetic immunity | $H_{PF}$ | | 1500 | | A/m | 50 Hz / 60 Hz |
| Pulse magnetic field immunity | $H_{PM}$ | | 2000 | | A/m | $t_p$ = 8 µs |
| Damped oscillatory magnetic field | $H_{OSC}$ | | 2000 | | A/m | 0.1 Hz – 1 MHz |
| Cross-axis immunity multiplier[8] | $K_X$ | | 2.5 | | | |

### DC-DC Convertor

| $T_{min}$ to $T_{max}$ and $V_{DD1A}$ = 3.0 V to 3.6 V unless otherwise stated | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min.** | **Typ.** | **Max.** | **Units** | **Test Conditions** |
| Output voltage | $V_{DD2A}$ | 3 | 3.3 | 3.45 | V | $T_{min}$ to $T_{max}$; full $V_{DD1A}$ and $I_{DD2A}$ operating range |
| Output current | $I_{DD2A}$ | 80 | | | mA | |
| Short-circuit protection limited current | | 115 | 125 | 135 | mA | |
| Input quiescent supply current | $I_{DD1AQ}$ | | 200 | 240 | mA | $I_{DD2A}$ = 0 |
| Input supply current | $I_{DD1A}$ | | 380 | 440 | mA | $I_{DD2A}$ = 80 mA |
| Line regulation | $\Delta V_{DD2A}/\Delta V_{DD1A}$ | | 32 | 40 | mV/V | 25 °C |
| | | | 16 | | mV/V | 125 °C |
| Load regulation | $\Delta V_{DD2A}/V_{DD2A}$ | | 5 | 6 | % | $I_{DD2A}$ = 0 to max. |
| Output voltage temperature coefficient | $(\Delta V_{DD2A}/V_{DD2A})/\Delta T$ | | 0.017<br>0.03 | | %/C | $I_{DD2}$ = 10 mA<br>$I_{DD2}$ = 50 mA |
| Capacitive load | $C_{DD2A}$ | | | 1000 | µF | |
| Output voltage ripple | $V_{DD2BRIPPLE}$ | | | 5 | $mV_{P-P}$ | 20 MHz bandwidth; $I_{DD2A}$ = max. |
| | | | 1 | | $mV_{P-P}$ | 1 kHz bandwidth; $I_{DD2A}$ = max. |
| Start-up time | $t_{SU}$ | | 200 | | µs | No load |
| | | | 400 | | µs | Full load ( resistive) |
| Convertor frequency | $f_{OSC}$ | 105 | 113 | 120 | MHz | |

## Shutdown Specifications

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| DC-DC convertor Overcurrent threshold | $I_{DD2A}$ | | 120 | | mA | |
| Brownout threshold voltage | $V_{DD2B}$ | | 2.5 | | V | Power-up |
| | | | 2.3 | | | Power-down |
| Bus driver shutdown temperature | $T_J$ | | 140 | | °C | Junction Temperature |
| Bus driver re-enable temperature | | | 135 | | | |

## Isolation Specifications

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Creepage distance (external) | | 8.03 | 8.3 | | mm | Per IEC 60601 |
| Total barrier thickness (internal) | | 0.013 | 0.016 | | mm | |
| Barrier resistance | $R_{IO}$ | | $>10^{14}$ | | Ω | 500 $V_{RMS}$ |
| Barrier capacitance | $C_{IO}$ | | 7 | | pF | f = 1 MHz |
| Leakage current | | | 0.2 | | $\mu A_{RMS}$ | 240 $V_{RMS}$, 60 Hz |
| Comparative tracking index | CTI | ≥600 | | | $V_{RMS}$ | Per IEC 60112 |
| Barrier life | | | 44000 | | Years | 100°C, 1000 $V_{RMS}$, 60% CL activation energy |

## Thermal Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions |
|---|---|---|---|---|---|---|
| Junction–ambient thermal resistance | $\theta_{JA}$ | | 67 | | °C/W | Double-sided PCB with thermal vias in free air |
| Junction–case (top) thermal resistance | $\theta_{JC}$ | | 12 | | °C/W | Double-sided PCB with thermal vias in free air |
| Junction–ambient thermal resistance | $\theta_{JA}$ | | 46 | | °C/W | 2s2p PCB with thermal vias per JESD51 with thermal vias in free air |
| Junction–case (top) thermal resistance | $\theta_{JC}$ | | 9 | | °C/W | 2s2p PCB with thermal vias per JESD51 with thermal vias in free air |
| Power dissipation | $P_D$ | | | 1.5 | W | |

## Notes:

1. Absolute Maximum specifications mean the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. Differential input/output voltage is measured at the noninverting terminal A with respect to the inverting terminal B.
3. $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of $V_{OD}$ and $V_{OC}$, respectively, that occur when the input is changed from one logic state to the other.
4. Includes 10 ns read enable time. Maximum propagation delay is 25 ns after read assertion.
5. Pulse skew is defined as $|t_{PLH} – t_{PHL}|$ of each channel.
6. Skew limit is the maximum propagation delay difference between any two devices at 25°C.
7. The relevant test and measurement methods are given in the “High Magnetic Immunity” section on p. 11.
8. External magnetic field immunity is improved by this factor if the field direction is “end-to-end” rather than to “pin-to-pin” (see diagram on p. 13).

## Device Operation

The IL4685 / IL4622 detailed block diagram is shown below. The major elements are a DC-DC convertor, an RS-485 / RS-422 transceiver, and GMR isolation:

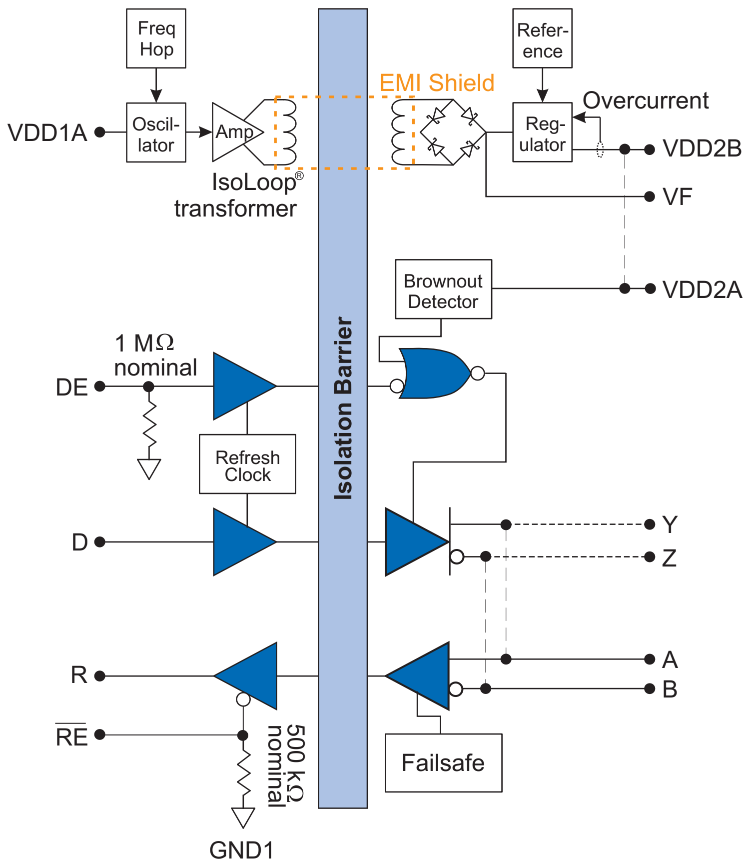



**Figure 1. IL4685 / IL4622 detailed block diagram.**

### DC-DC Convertor Operation

A 113 MHz oscillator drives a high-frequency power amplifier, which in turn drives an IsoLoop® microtransformer primary. Frequency hopping reduces EMI peak amplitudes, and embedded magnetic shielding further reduces radiated EMI.

A unique ceramic/polymer composite barrier provides full 2.5 kV isolation with virtually unlimited barrier life.

On the other side of the isolation barrier, the transformer secondary output is filtered, rectified, and regulated by a low-EMI low drop-out regulator with a precision bandgap voltage reference.

*Simple Capacitive Decoupling*

The only external parts required are a 0.1 µF capacitor placed as close as possible to the VDD1B supply pin, a 10 µF ceramic capacitor for the VDD2 or VDD2B pin, and a 0.1 µF/16 V filter capacitor near the $V_F$ pin. This low external parts count reduces board area and cost.

*Short-Circuit Protection*

The DC-DC convertor output will shut down at a current of approximately 120 mA. Short-circuit protection automatically resets and the output recovers when the fault is removed.

### Transceiver Operation

*Receiver Features*

The receiver output “R” has tri-state capability via the active low $\overline{\text{RE}}$ input.

*Driver Features*
The driver features low propagation delay skew to maximize bit width and minimize EMI. Drivers have tri-state capability via the active-high DE input.

*True 3.3-volt Bus Operation*
IL46xx parts are guaranteed to provide the minimum RS-485 / RS-422 differential voltages with a 3.0-volt bus supply, providing true 3.3-volt bus operation with ample design margins.

*Deterministic Power Up and Brownout Detection*
IL46xx parts have circuitry to disable the transceiver bus until the driver-side voltage (VDD2B, normally provided by the DC-DC convertor) reaches approximately 2.5 volts on power-up. The transceiver is disabled when the voltage drops below approximately 2.3 volts on power-down. This brownout circuitry ensures the transceiver does not "crash" the bus on power up, power down, or brownout, and eliminates the need for external power supply monitors. In addition, a patented refresh circuit maintains the correct transceiver output state with respect to data input (DC correctness). The refresh circuit ensures the bus outputs will follow the Function Table shown on Page 1 after power up.

*Hot Plug Operation*
Deterministic power-up allows IL46xx nodes to "hot plug" into the bus, since the bus driver will be in a high-impedance state until the DC-DC convertor output is enough for the bus driver to operate.

*Unpowered Nodes*
The bus driver reverts to high impedance when VDD2 is not present, so that unpowered nodes do not disturb bus operation.

*Full Fail-Safe*
The receiver is full fail-safe, meaning it guarantees a forces a logic high state on "R" if the "A" and "B" bus inputs are unconnected, shorted together, or connected to a terminated bus with all the transmitters disabled (terminated/undriven).

*Thermal Shutdown*
The bus driver is disabled when the driver die temperature exceeds approximately 150 °C, and re-enabled when the die temperature drops below approximately 135°C. The receiver and DC-DC convertor sections continue to operate during thermal shutdown.

**Internal Connections**

*Ground Connections*
There are two pins for each ground connection: pin 2 is internally connected to pin 8 and pin 15 is internally connected to pin 9.

*Power Connections*
The controller-side DC-DC convertor and transceiver functions have separate power connections, VDD1A and VDD1B respectively, which should be connected externally for normal operation. The bus-side DC-DC convertor and transceiver functions have separate power connections (VDD2A and VDD2B) in the IL4685. The bus-side DC-DC convertor and transceiver functions are internally connected in the IL4622.

*Bus Connections*
The IL4685 has a half-duplex transceiver generally used with RS-485. Bus input "A" is internally connected to "Y" and "B" connected to "Z." The IL4622 has full-duplex connections for RS-422 busses. For a half duplex RS-485 network with the IL4622, "A" can be externally connected to "Y," and "B" connected to "Z."

**GMR Isolator Operation**

An equivalent circuit for each of the Giant Magnetoresistor (GMR) isolator channels is shown in Figure 2:

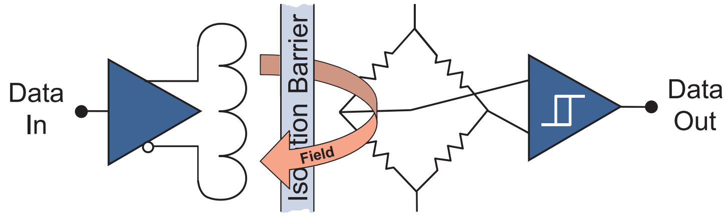



**Figure 2. Isolator model signal path.**

The GMR isolator signal path starts with a buffered input signal that is driven through an ultraminiature coil. This generates a small magnetic field that changes the electron spin polarization of GMR resistors, which are configured as a Wheatstone bridge. The change in spin polarization of the resistors creates a bridge voltage which drives an output comparator to construct an isolated version of the input signal. GMR is inherently high speed and low distortion.

**High Magnetic Immunity**
GMR provides large signals which improve magnetic immunity, and the Wheatstone bridge configuration cancels ambient common-mode magnetic fields, further enhancing immunity to external magnetic fields.

## Thermal Management

An IL46xx transceiver node can be operated at worst-case loading, data rate, and ambient temperature without exceeding the maximum DC-DC convertor output current, maximum die temperature or package power rating. As shown in Figure 18, worst-case power consumption for a node such as that shown in Figure 20 is less that 1.2 watts. Junction-to-ambient thermal resistance is 46 °C/W with a 2s2p circuit board, so the temperature rise is 55 °C and the die temperature is within the 140 °C maximum at the 85 °C maximum ambient.

If additional nodes are powered by the DC-DC convertor or additional power is needed from the DC-DC convertor, however, care should be taken to ensure the die temperature does not exceed its 140 °C maximum operating temperature, and that the total power dissipation does not exceed the 1.5 watt package maximum. The following sections summarize some thermal management considerations in these situations.

***Board Layout***

If possible, use a double sided, double buried power plane ("2s2p") board to maximize thermal performance. Thermal vias should be used between the power plane and the board surfaces. All four IC ground pins should be connected, with wide traces to help cool the leadframe.

***Use Low-Power, Fractional-Load Transceivers***

Transceivers such as the NVE IL3685P are fractional load to minimize the drive current required by transmitting nodes and, if powered by the IL46xx, uses less bus power than other transceivers.

***Avoid Termination Resistors with Shorter Bus Cables***

Termination resistors minimize reflections, which can be important for long cable lengths. However, these resistors significantly increase output drive current and may not be necessary with short bus cables.

***Full Duplex Uses Less Power***

Full-duplex RS-422 buses have only one transmitter per bus and therefore only need one termination resistor, typically 120 Ω. Half-duplex RS-485 networks with long cables, however, are generally terminated on both ends because either end can receive data. This doubles the power dissipated in the termination resistors.

***No External "Fail-Safe" Resistors***

The transceivers are designed to be "full fail-safe," so "fail-safe" pull-up and pull-down bias resistors are generally unnecessary, and use power.

***Minimize Data Rate***

The transceiver draws more power at higher frequency, so the data rate should not be higher than necessary to minimize transceiver power.

***Limit Transmission Time***

The transceivers use less power receiving than transmitting, and much less if there are termination resistors. Average power dissipation can be reduced considerably by disabling the driver (DE = LOW) when not transmitting data.



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## Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

## Inherently Low EMI

IL46xx parts designed for compliance with IEC 61000-6-3, IEC 61000-6-4, CISPR, and FCC Class A standards for emissions.

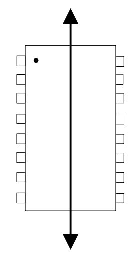
The DC-DC convertor oscillator operates above 88 MHz, where emission limits are higher since there is less risk of interference with common commercial radio and television broadcasting.

Frequency-hopping technology dramatically reduces peak EMI, and synchronous rectification and PWM control are avoided, resulting in inherently low EMI. Ferrite beads are generally not required for EMI mitigation.

## High Magnetic Immunity

These parts are fully compliant with IEC 61000-6-1 and IEC 61000-6-2 magnetic immunity standards.

The IsoLoop Isolator's Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EM immunity. Immunity to external magnetic fields is even higher if the field direction is "end-to-end" (rather than to "pin-to-pin") as shown at right.



## Typical Performance Graphs

The following graphs show typical performance:

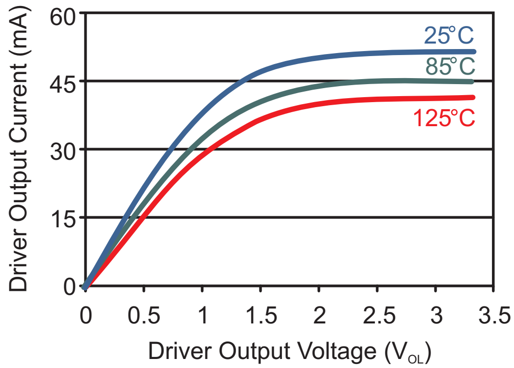



**Figure 3. Typ. driver output current vs. driver output voltage ($V_{OL}$).**

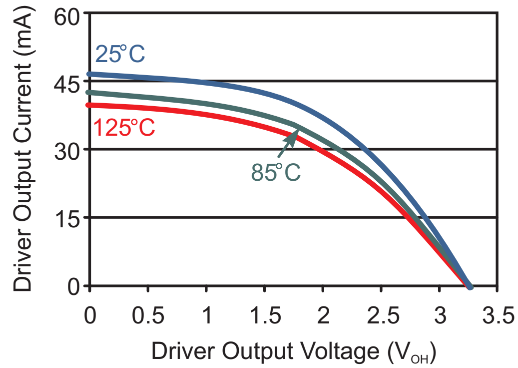



**Figure 4. Typ. driver output current vs. driver output voltage ($V_{OH}$).**

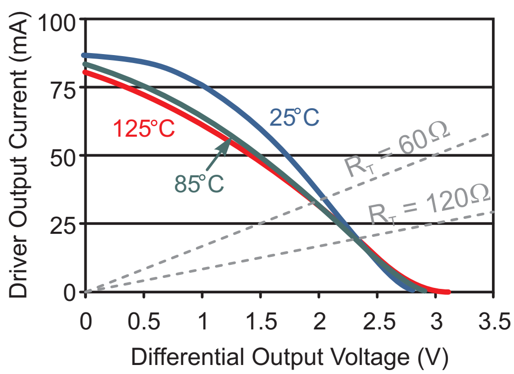



**Figure 5. Typical transceiver differential output versus driver output current.**

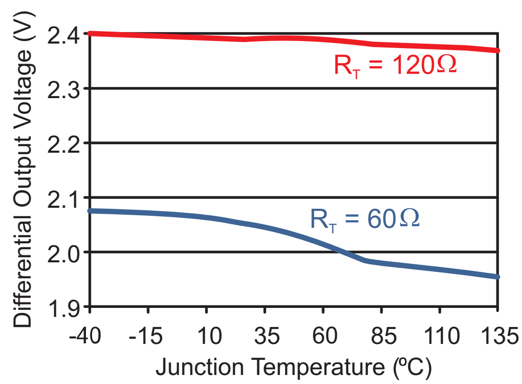



**Figure 6. Typical transceiver differential output versus temperature.**

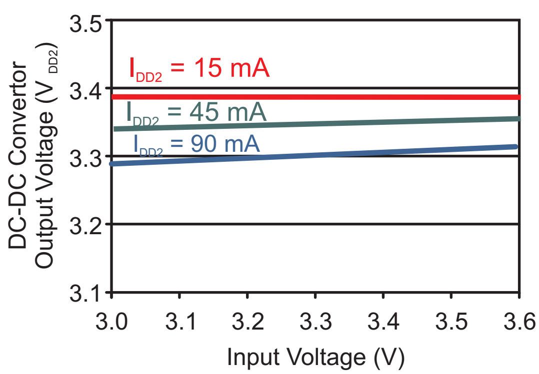



**Figure 7. Typical DC-DC convertor line regulation.**

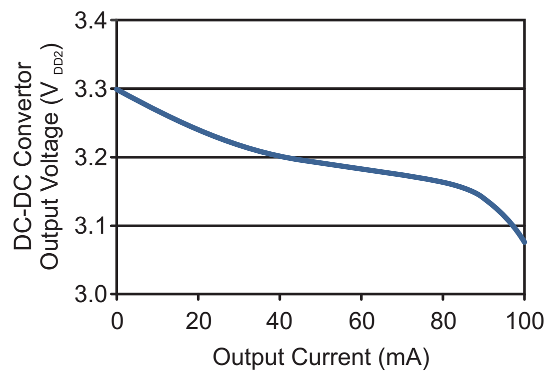



**Figure 8. Typical DC-DC convertor load regulation ($V_{DD1A}$ = 3.3 V).**

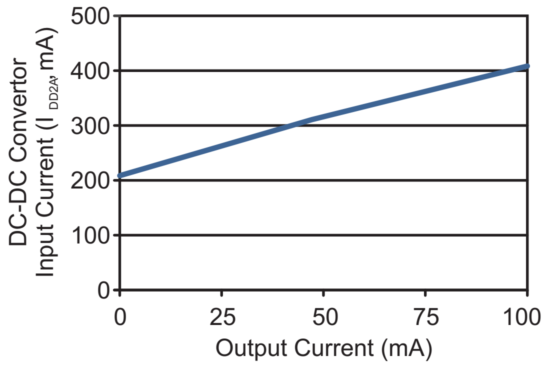



**Figure 9. Typ. DC-DC convertor supply current vs. output current ($V_{DD1A}$ = 3.3 V).**

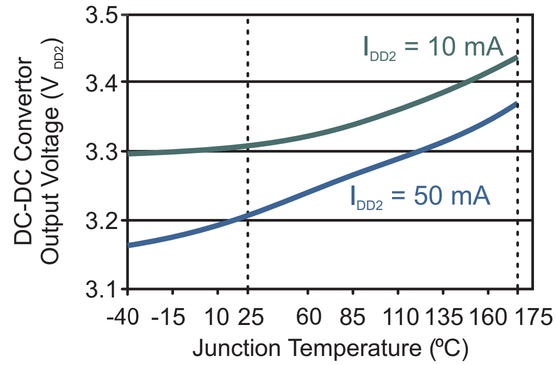



**Figure 10. Typical DC-DC convertor output versus temperature ($V_{DD1A}$ = 3.3 V).**

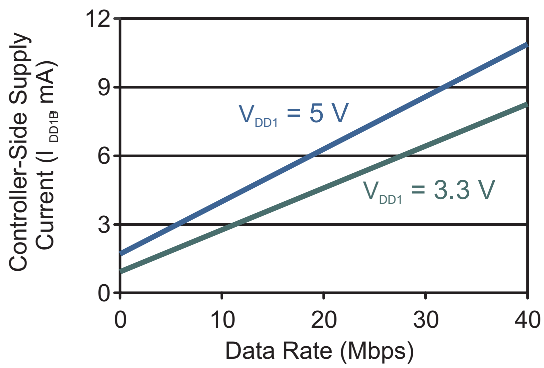



**Figure 11. Transceiver controller-side supply current versus data rate.**

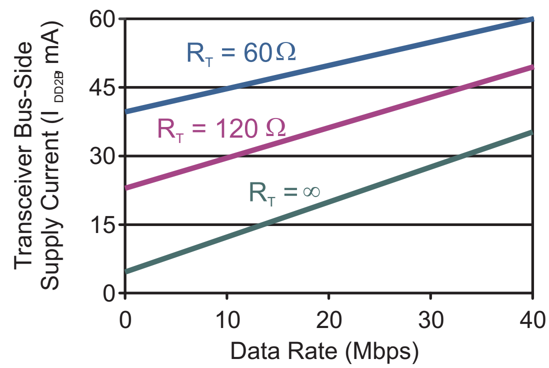



**Figure 12. Typical transceiver bus-side supply current ($I_{DD2}$) versus aggregate termination resistance ($V_{DD2}$ = 3.3 V).**

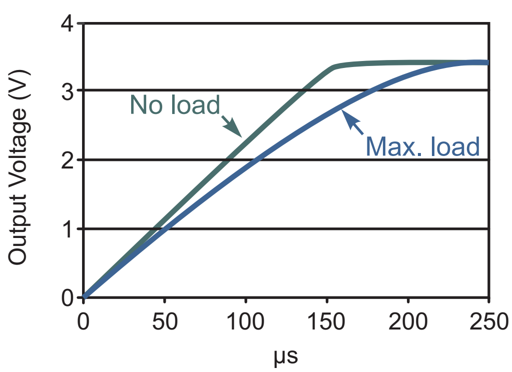



**Figure 13. Typical DC-DC convertor startup.**

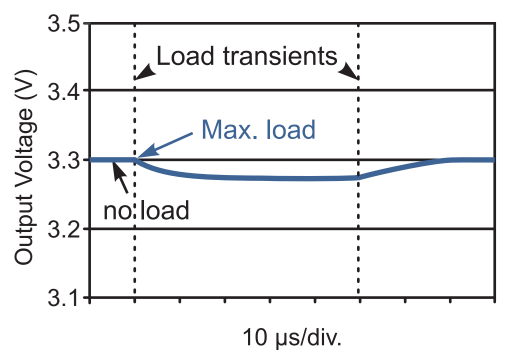



**Figure 14. DC-DC convertor transient response.**



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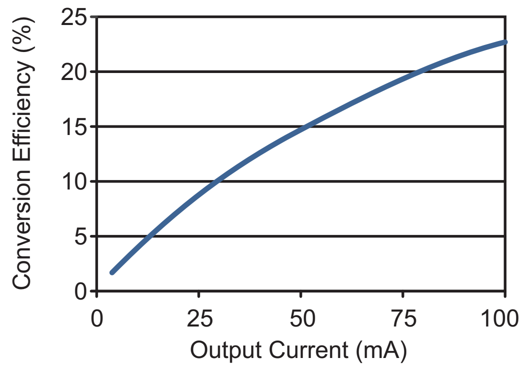



**Figure 15. Typ. DC-DC convertor power efficiency ($V_{DD1}$ = 3.3 V; 25 °C).**

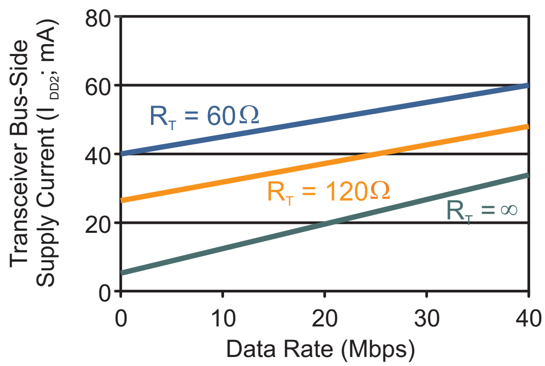



**Figure 16. Typical transceiver bus-side supply current ($I_{DD2}$) versus operating speed.**

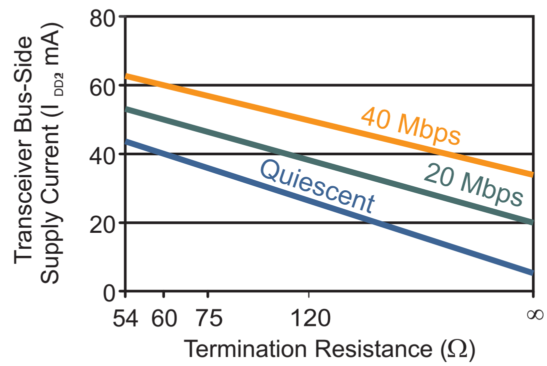



**Figure 17. Typ. transceiver bus-side supply current ($I_{DD2}$) vs. aggregate termination resistance.**

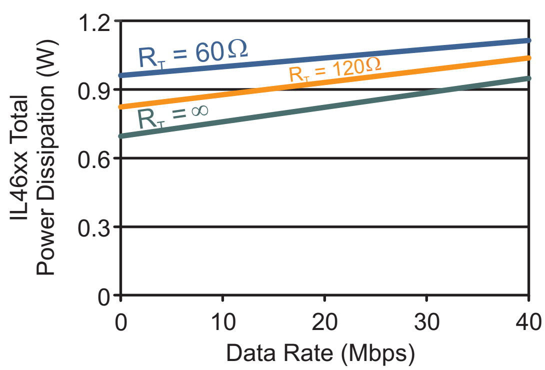



**Figure 18. Total power dissipation versus operating speed ($V_{DD1A}$ = $V_{DD1B}$ = 3.3 V; $V_{DD2A}$ connected to $V_{DD2B}$).**

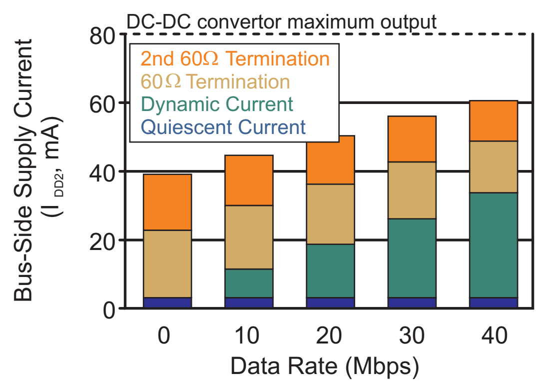



**Figure 19. IL46xx bus-side supply current budget.**

## Application Information

IL46xxEs form complete, isolated, independent bus nodes. Termination resistors are optional.

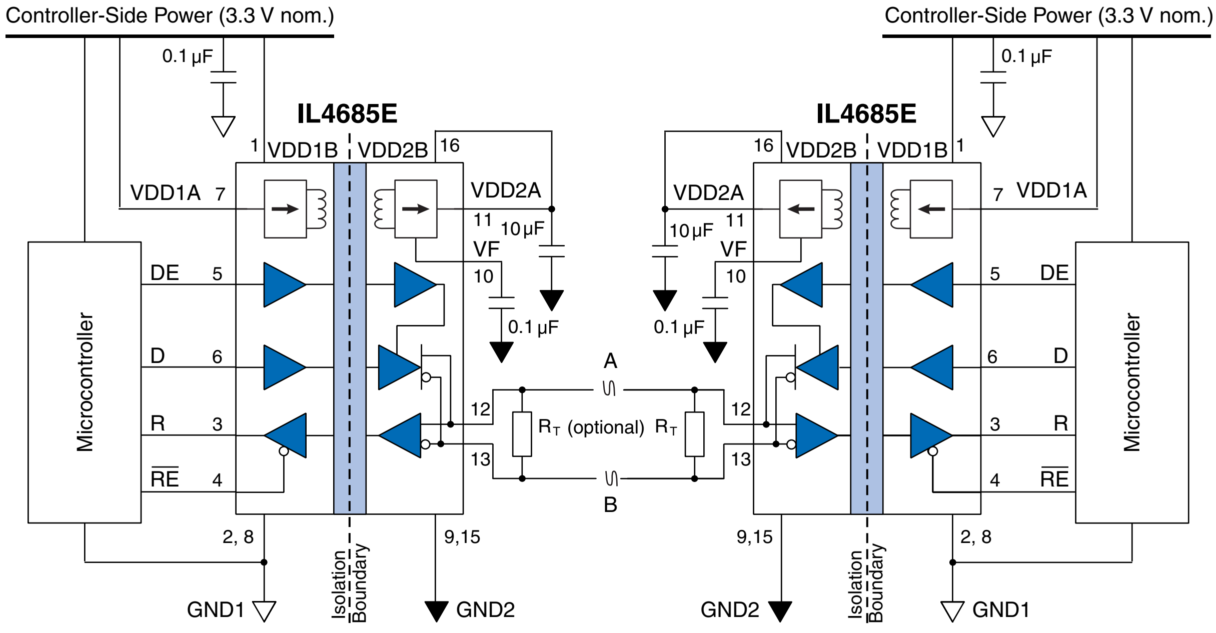



**Figure 20. Two typical IL4685E nodes.**

An IL46xxE can drive five-volt or 3.3-volt nodes. Termination resistors are optional.

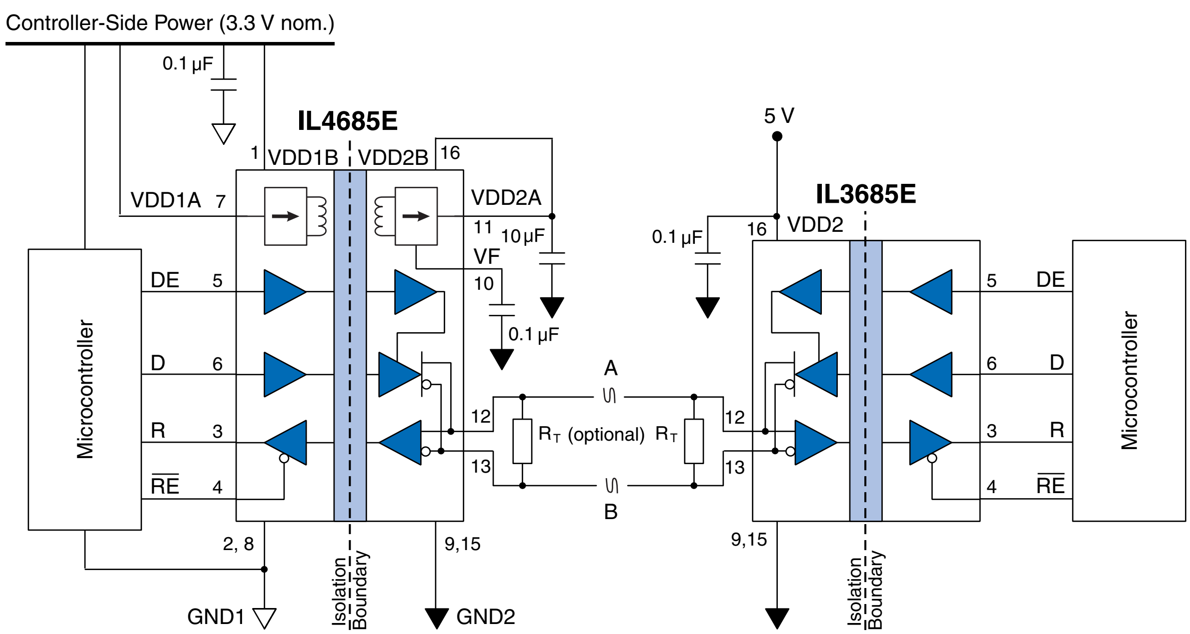



**Figure 21. A typical IL4685E node driving a 5-volt-powered node.**

IL4622Es can be used to create full-duplex RS-422 networks where one node broadcasts and multiple nodes can receive.

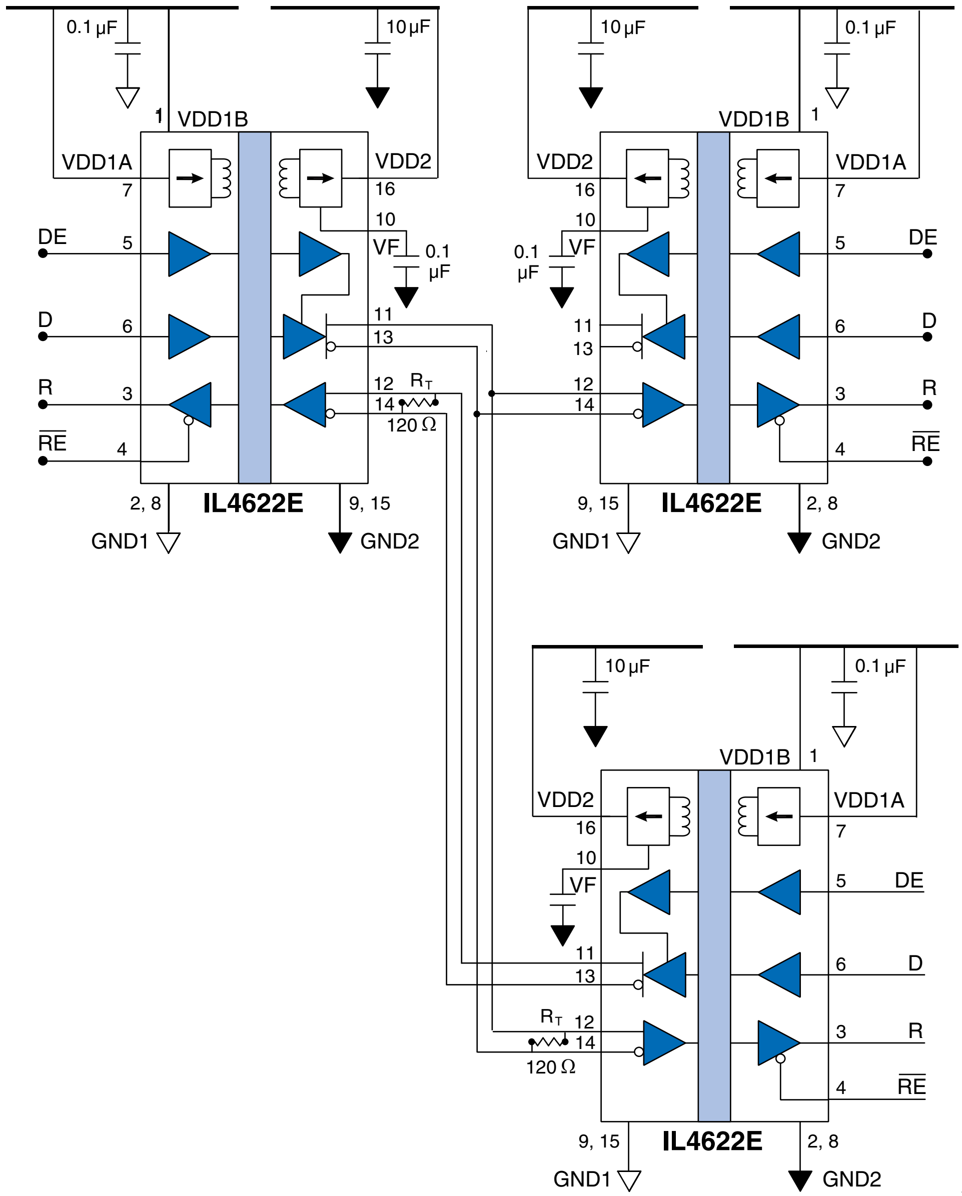



**Figure 22. A full-duplex multi-drop RS-422 network.**

The IL46xxE integrated DC-DC convertor produces enough current to power multiple bus nodes. Isolated transceivers provide isolation from the bus. In the circuit below, the IL3685PE isolated transceiver uses the same transceiver circuitry as the IL4685E, and is fully-compatible with the 3.3-volt bus power and has a 1/5 unit load to minimize bus power. Termination resistors are not used to minimize power consumption.

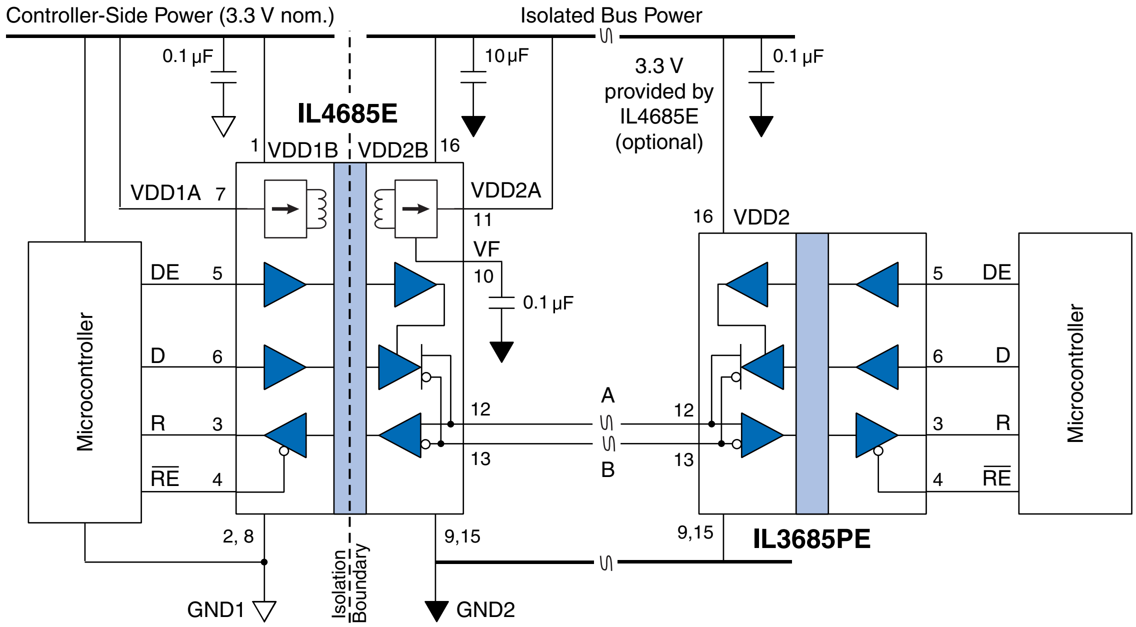



**Figure 23. IL4685E powered bus with two fully-isolated nodes. The IL4685E powers both nodes.**

If double isolation is not required, a non-isolated 3.3-volt transceiver such as the ISL3179E can be used. The IL4685 can power the remote node if desired:

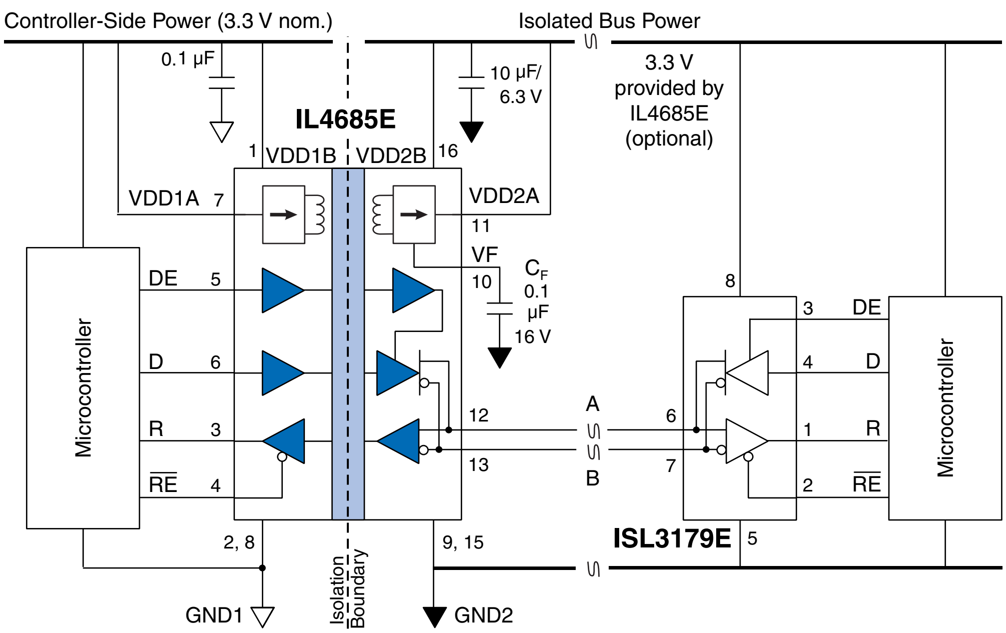



**Figure 24. IL4685E powered bus with a non-isolated node.**

## Evaluation Board

The IL4622-01 Evaluation Board provides a complete isolated RS-485 or RS-422 node using the IL4622.

The 4 by 3 inch (100 x 75 mm) board provides uses a 2s2p board with thermal vias to optimize thermal performance. There are screw terminals for bus connections and test points for checking voltages and waveforms. Jumpers allow the board to be used as full duplex (separate A/B bus receiver from the Y/Z bus driver connections), or half duplex ("A" jumpered to "Y" and "B" jumpered to "Z"). Each board has a place for a bus termination resistor.

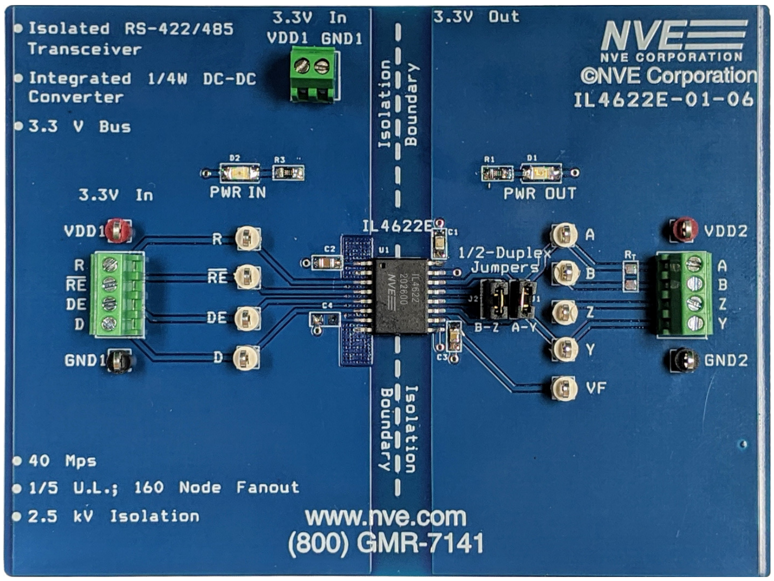
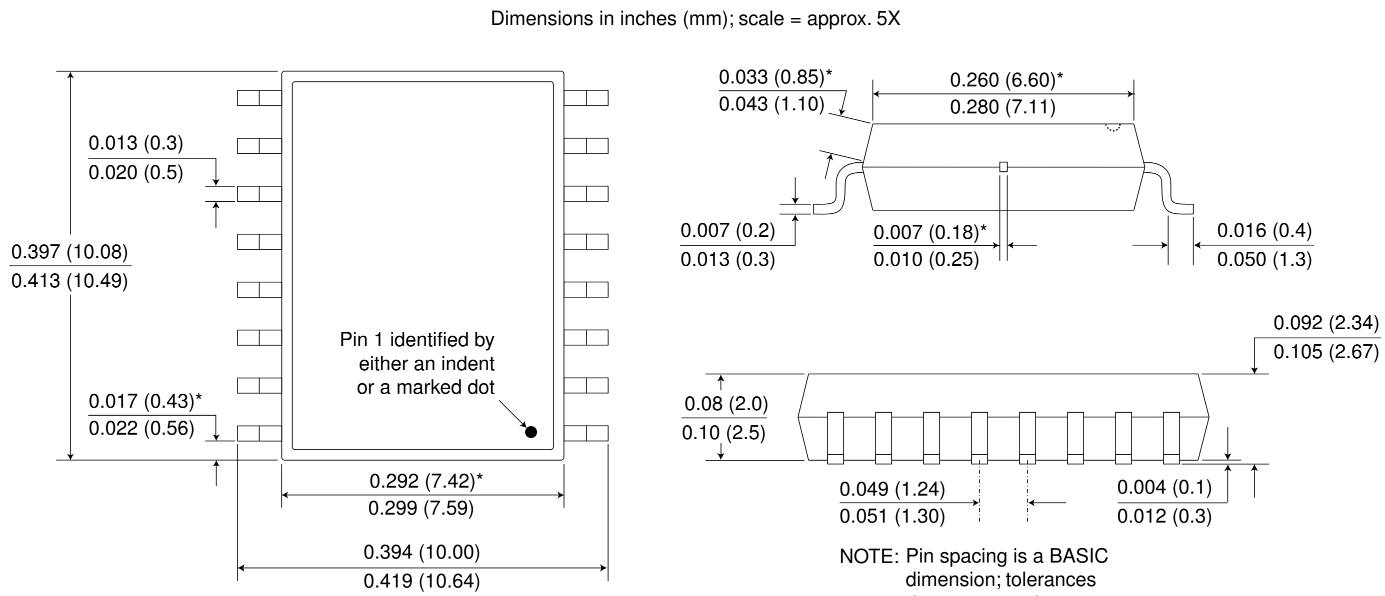


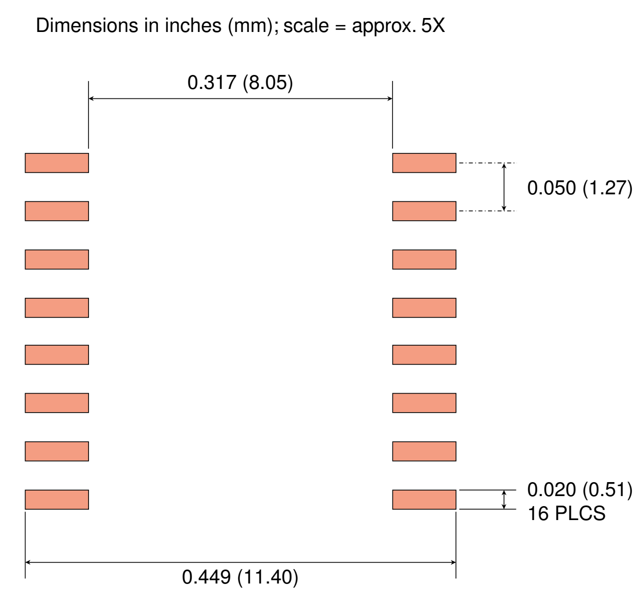

**Figure 25. IL4622-01 Evaluation Board (actual size).**

## Package Drawing




*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

## Recommended Pad Layout



## Available Part Numbers

| Part Number | Bus | Duplex | Bulk Packaging | RoHS? |
|---|---|---|---|---|
| IL4622E | RS-422 / RS-485 | Full | Tubes (50 pcs.) | RoHS |
| IL4685E | RS-485 | Half | | |
| IL4622E-TR7 | RS-422 / RS-485 | Full | 7-inch reels (up to 450 pcs.) | |
| IL4685E-TR7 | RS-485 | Half | | |
| IL4622E-TR13 | RS-422 / RS-485 | Full | 13-inch reels (up to 1500 pcs.) | |
| IL4685E-TR13 | RS-485 | Half | | |
| IL4622 | RS-422 / RS-485 | Full | Tubes (50 pcs.) | SnPb finish (non-RoHS; Special Order) |
| IL4685 | RS-485 | Half | | |
| IL4622-TR7 | RS-422 / RS-485 | Full | 7-inch reels (up to 450 pcs.) | |
| IL4685-TR7 | RS-485 | Half | | |
| IL4622-TR13 | RS-422 / RS-485 | Full | 13-inch reels (up to 1500 pcs.) | |
| IL4685-TR13 | RS-485 | Half | | |

## Revision History

| | |
|---|---|
| **ISB-DS-001-IL46xx-RevA**<br>**July 2020** | **Changes**<br>• Initial release.<br>• Table corrections and final specifications (pp. 3 – 8).<br>• Changed IL4622E pinout (p. 5).<br>• Specification notes (p. 8).<br>• Added electrical fast transient (EFT) specification per IEC61000-4-4 for bus nodes (p. 3).<br>• Added overcurrent protection to DC-DC convertor detailed block diagram (Fig. 3).<br>• Added Shutdown Specifications table (p. 7).<br>• Added detailed block diagram (Fig. 1) and GMR isolator diagram (Fig. 2).<br>• More details on power up, hot plug, brownout detection, and unpowered nodes (p. 10).<br>• Added and finalized performance graphs (pp. 14 – 16).<br>• Added 120 Ω aggregate termination resistance (common for RS-422) to performance graphs.<br>• Added RS-422 application diagram (Figure 21). |
| **ISB-DS-001-IL46xx-PRELIM4**<br>**March 2020** | **Changes**<br>• Added full-duplex version (IL4622E).<br>• Increased Working Voltage to 700 $V_{RMS}$ based on final VDE data.<br>• Rearranged application information text.<br>• Additional application circuits.<br>• Added evaluation board. |
| **ISB-DS-001-IL4685-PRELIM3**<br>**December 2019** | **Changes**<br>• Increased DC-DC convertor output power.<br>• Additional DC-DC convertor specifications.<br>• Performance graphs.<br>• Two-node application circuits.<br>• Changed external capacitor values. |
| **ISB-DS-001-IL4685-PRELIM2**<br>**November 2018** | **Changes**<br>• Replaced text in block diagram with arrows.<br>• Minor text revisions. |
| **ISB-DS-001-IL4685-PRELIM**<br>**October 2018** | **Change**<br>• Preliminary release. |

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*July 2020*