

Datasheet

Veda™ IF912

Version 0.5

Revision History

Version	Date	Notes	Contributors	Approver
0.1	13 May 2025	Preliminary release	Andrew Chen	Andy Ross
0.2	22 May 2025	Section 4: Update Storage humidity range to 5%~95%. Operating humidity range < 85%. Section 6: Update the SDIO/gSPI pin details. Section 7.2: Correct the schematic drawing on SMIF connection (Chip select pin) with external NOR and PSRAM.	Andrew Chen	Andy Ross
0.3	20 June 2025	Correct the pin define on pin 82-83	Andrew Chen	Andy Ross
0.4	14 July 2025	Update RF performance	Andrew Chen	Andy Ross
0.5	16 Sep 2025	Corrected to reflect that Bluetooth does not support BR/EDR	Andrew Chen	Andy Ross

Contents

1	Scope.....	4
2	Introduction.....	4
2.1	General Description.....	4
3	Veda IF912 Series Feature Summary	6
4	Specifications	7
5	Block Diagrams.....	12
5.1	Veda IF912 module Block Diagram	12
6	Pin Definitions.....	13
7	Veda IF912 Implementation Details	17
7.1	Power up sequency timing.....	17
7.2	L-C filter for Buck switching regulator	17
7.3	Serial Memory Interface (SMIF) Connection.....	18
7.4	SDIO and gSPI strapping configuration	20
7.4.1	SDIO mode.....	20
7.4.2	gSPI mode	20
7.5	MHF4 and Embedded PCB antenna	21
8	Mechanical Specifications.....	22
9	Material handling information	23
9.1	Required Storage Conditions	23
9.1.1	Prior to Opening the Dry Packing	23
9.1.2	After Opening the Dry Packing	23
9.1.3	Temporary Storage Requirements after Opening	23
9.2	Baking Conditions.....	24
10	Surface Mount Conditions.....	25
10.1	Recommended Stencil Aperture.....	25
10.2	Soldering profile.....	25
11	Cautions When Removing the SIP from the Platform for RMA.....	26
11.1.1	Precautions for Use.....	26
12	Certified Antennas.....	27
13	Additional Information	28

1 Scope

This document describes key hardware aspects of the Ezurio Veda™ IF912 series wireless modules which is a ultra-lower power, single chip connected MCUs with 1x1 Wi-Fi 6 dual band, Bluetooth® Low Energy 5.4, Matter and IP networking. Integrated MCU, Radio, PMU, Flash and PSRAM in 11x7mm size that targeted at Internet-of- Things (IoT) applications for stand-alone operation or to offload a host-processor.

This document is intended to assist device manufacturers and related parties with the integration of this radio into their host devices. Data in this document is drawn from several sources and includes information found in the Infineon CYW55912 Reversion C 2024-10-30 data sheet, along with other documents provided by Infineon.

Note: The information in this document is subject to change. Please contact Ezurio to obtain the most recent version of this document.

2 Introduction

2.1 General Description

The Veda IF912 series wireless module is a highly integrated, small form factor Wi-Fi/Bluetooth module that is optimized for low-power mobile devices, featuring:

- **MCU:** 192 MHz Arm® Cortex®-CM33, runs the Wi-Fi and Networking Stacks.
- **Memory:**
 - On-Chip memory: 2048-KB ROM and 768-KB RAM. (No Embedded Memory variant)
 - Embedded external memory: 8M PSRAM, 8M Flash. (Embedded Memory, 8M PSRAM, 8M Flash variant)
 - **Note: For other embedded memory size, please contact Ezurio.**
- **Wi-Fi:**
 - 1X1, IEEE 802.11a/b/g/n/ac/ax compliant.
 - Dual-band (2.4/5GHz), 20 MHz channels supporting PHY data rates up to 802.11ax (MCS11 1024-QAM 5/6).
 - Transmit (TX) power with internal PA and LNA.
 - Wi-Fi 6 release feature:
 - OFDMA uplink and downlink as STA
 - Downlink multi-user MIMO as STA
 - Individual target-wake-time (TWT)
- **Bluetooth®:**
 - Bluetooth® 5.4 (Bluetooth® Low Energy)
 - Advertising Coding Selection
 - Encrypted Advertising Data
 - LE Generic Attribute Profile (GATT) Security Levels Characteristic
 - Bluetooth® Low Energy 5.0/5.1/5.2/5.3 features
 - LE long range
 - LE 2 Mbps
 - LE mesh
 - Advertising extensions
- **Security:**
 - Arm® Trustzone Cryptocell 312
 - Life cycle management
 - Crypto key establishment and management Crypto offloads
 - Secure boot
 - Wi-Fi and Bluetooth® independent firmware authentication
 - Firmware encryption
 - Attestation
 - Anti-rollback prevention

The Veda IF912 integrated with all WLAN and Bluetooth functionality in a small package supports a low cost and simple implementation. The radio is pre-calibrated and integrates the complete transmit/receive RF paths including bandpass filter, diplexer, switches, reference crystal oscillator, and power management units (PMU). It is available in **7x11x1.4mm solder-down LGA form factors** with an RF trace pin out for both Wi-Fi and BT.

A reference certified embedded PCB antenna or the implementation of MHF4 connector for external antennas are available on Veda IF91x DVK, please contact Ezurio for detail information. A list of certified external antennas is shown in **Error! Reference source not found..**

Ordering information is listed in **Table 1**. Please contact Ezurio Sales/FAE for further information.

Table 1: Product ordering information

Part Number	Description
453-00396R	Module, Veda IF912, SIP, Dual Band, No Embedded Memory, RF Trace Pin, Tape and Reel
453-00396C	Module, Veda IF912, SIP, Dual Band, No Embedded Memory, RF Trace Pin, Cut Tape
453-00397R	Module, Veda IF912, SIP, Dual Band, Embedded Memory, 8M PSRAM, 8M Flash, RF Trace Pin, Tape and Reel
453-00397C	Module, Veda IF912, SIP, Dual Band, Embedded Memory, 8M PSRAM, 8M Flash, RF Trace Pin, Cut Tape
453-00396-K1	Development Kit, Module, Veda IF912, SIP, Dual Band, External Memory, RF Trace Pin

3 Veda IF912 Series Feature Summary

The Ezurio Veda IF912 series device features are described in [Table 2](#).

Table 2: Veda IF912 series wireless module feature

Feature	Description																											
Radio Front End	- Integrates the complete transmit/receive RF paths including bandpass filter, diplexer, switches, reference crystal oscillator, and power manage unit (PMU) - Supports dual-band (2.4/5 GHz) - Supports 20MHz channel bandwidth - Supports 1x1 WLAN/Bluetooth antenna configuration																											
The <i>Bluetooth</i>[®] word mark and logos are registered trademarks owned by Bluetooth SIG, Inc. Any use of such marks by Ezurio is under license. Other trademarks and trade names are those of their respective owners. One buck regulator, multiple LDO regulators, and a power management unit (PMU) are integrated into the Veda IF913. All regulators are programmable via the PMU. These blocks simplify power supply design for Bluetooth and WLAN functions in embedded designs.																												
Pre-Calibration	RF system tested and calibrated in production																											
Sleep Clock	Internal low-power oscillator accuracy is only adequate for WLAN, and not for Bluetooth[®], if low power for Bluetooth[®]Low-Energy required. External 32.768 KHz sleep clock is required for Bluetooth[®] Low Energy to support low power mode. The 32.768 kHz precision oscillator which meets the requirements listed following table must be used. <table><tr><th>Parameter</th><th>LPO Clock</th><th>Unit</th></tr><tr><td>Nominal input frequency</td><td>32.768</td><td>kHz</td></tr><tr><td>Frequency accuracy</td><td>±250</td><td>ppm</td></tr><tr><td>Duty cycle</td><td>30 – 70</td><td>%</td></tr><tr><td>Input signal amplitude</td><td>200 – 3300</td><td>mV, p-p</td></tr><tr><td>Signal type</td><td>Square-wave or sine-wave</td><td>-</td></tr><tr><td>Input impedance</td><td>> 100k</td><td>Ω</td></tr><tr><td></td><td>< 5</td><td>pF</td></tr><tr><td>Clock jitter (during initial startup)</td><td>< 10,000</td><td>ppm</td></tr></table>	Parameter	LPO Clock	Unit	Nominal input frequency	32.768	kHz	Frequency accuracy	±250	ppm	Duty cycle	30 – 70	%	Input signal amplitude	200 – 3300	mV, p-p	Signal type	Square-wave or sine-wave	-	Input impedance	> 100k	Ω		< 5	pF	Clock jitter (during initial startup)	< 10,000	ppm
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Advanced WLAN	- IEEE 802.11a/b/g/n/ac/ax compliant, tri-band capable (2.4/5 GHz) 1x1 MIMO providing up to 143 Mbps PHY data rate for 2.4/5 GHz (1024-QAM modulation) - Supports 20 MHz bandwidth with optional SGI (1024-QAM modulation) - On-chip power amplifiers and low-noise amplifiers for both bands - Support wide variety of WLAN encryption: WPA2(Personal/Enterprise), WPA3 (Personal/Enterprise with 192 bit security).																											
Advanced Bluetooth	- Bluetooth[®] 5.4 (Bluetooth[®] Low Energy) - Advertising Coding Selection - Encrypted Advertising Data - LE Generic Attribute Profile (GATT) Security Levels Characteristic - Bluetooth[®] Low Energy 5.0/5.1/5.2/5.3 features - LE long range - LE 2 Mbps - LE mesh - Advertising extensions - Host controller interface (HCI) using a high speed UART and PCM/I2S for audio data - Low power consumption improves battery life of IoT and embedded devices																											

4 Specifications

Table 3: Specifications

Feature	Description
Physical size	11x7x1.4mm in 108-pin LGA package
Network communication interface	Secure Digital I/O 2.0 (1.8V only) /3.0; UART, gSPI, UART, SPI.
Main Chipset	Infineon AIROC™ CYW55912
Input Voltage Requirements	Typical DC 3.3 V, operating range from DC 3.13V to 4.8V
I/O Signalling Voltage	Typical DC 1.8 V ± 5%
Operating Temperature	-40° to +85°C (-40° to +185°F)
Operating Humidity	< 85% (non-condensing)
Storage Temperature	-40° to +85°C (-40° to +185°F)
Storage Humidity	5 to 95% (non-condensing)
MSL (Moisture Sensitivity Level)	4
Maximum Electrostatic Discharge	Conductive 8KV; Air coupled 12KV (follows EN61000-4-2)
Weight – g (oz.)	TBD
Network Architecture Types	Infrastructure (client operation)
Wi-Fi Standards	IEEE 802.11ax, 11ac, 11ac, 11a/b/g/n, 11d/h, 11i, 11r, 11w, 11e, 11k, 11ai, 11v
Bluetooth Standards	Bluetooth BLE 5.0, 5.1, 5.2, 5.3, 5.4
Wi-Fi Data Rates Supported	Support 802.11 ax/ac/a/b/g/n 1x1 MU-MIMO. 802.11b (DSSS, CCK) 1, 2, 5.5, 11 Mbps 802.11a/g (OFDM) 6, 9, 12, 18, 24, 36, 48, 54 Mbps 802.11n (OFDM, HT20, MCS0-7) 802.11ac (OFDM, VHT20, MCS0-8) 802.11ax (2.4 GHz / OFDM / HE20 / MCS0-11; 2.4 GHz / OFDMA / HE20 / MCS0-11) 802.11ax (5 GHz / OFDM / HE20 / MCS0-11; 5 GHz / OFDMA / HE20 / MCS0-11)

Feature	Description
Modulation Table	BPSK, QPSK, CCK, 16-QAM, 64-QAM, 256-QAM, 1024-QAM

Modulation Type						OFDM (IEEE 802.11n/ac)		OFDM (IEEE 802.11ax)		
MCS Index			Spatial Stream	Modulation	Coding	20MHz		20MHz		
HT	VHT	HE				0.8us GI	0.4us GI	0.8us GI	1.6us GI	3.2us GI
0	0	0	1	BPSK	1/2	6.5	7.2	8.6	8.1	7.3
1	1	1	1	QPSK	1/2	13	14.4	17.2	16.3	14.6
2	2	2	1	QPSK	3/4	19.5	21.7	25.8	24.4	21.9
3	3	3	1	16-QAM	1/2	26	28.9	34.4	32.5	29.3
4	4	4	1	16-QAM	3/4	39	43.3	51.6	48.8	43.9
5	5	5	1	64-QAM	2/3	52	57.8	68.8	65	58.5
6	6	6	1	64-QAM	3/4	58.5	65	77.4	73.1	65.8
7	7	7	1	64-QAM	5/6	65	72.2	86	81.3	73.1
	8	8	1	256-QAM	3/4	78	86.7	103.2	97.5	87.8
	9	9	1	256-QAM	5/6	N/A	N/A	114.7	108.3	97.5
		10	1	1024-QAM	3/4			129	121.9	109.7
		11	1	1024-QAM	5/6			143.4	135.4	121.9

OFDMA (IEEE 802.11ax)																
MCS Index	Spatial Stream	Modulation	Coding	26-tone RU			52-tone RU			106-tone RU			242-tone RU			
HE				0.8us GI	1.6us GI	3.2us GI	0.8us GI	1.6us GI	3.2us GI	0.8us GI	1.6us GI	3.2us GI	0.8us GI	1.6us GI	3.2us GI	
0	1	BPSK	1/2	0.9	0.8	0.8	1.8	1.7	1.5	3.8	3.5	3.2	8.6	8.1	7.3	
1	1	QPSK	1/2	1.8	1.7	1.5	3.5	3.3	3	7.5	7.1	6.4	17.2	16.3	14.6	
2	1	QPSK	3/4	2.6	2.5	2.3	5.3	5	4.5	11.3	10.6	9.6	25.8	24.4	21.9	
3	1	16-QAM	1/2	3.5	3.3	3	7.1	6.7	6	15	14.2	12.8	34.4	32.5	29.3	
4	1	16-QAM	3/4	5.3	5	4.5	10.6	10	9	22.5	21.3	19.1	51.6	48.8	43.9	
5	1	64-QAM	2/3	7.1	6.7	6	14.1	13.3	12	30	28.3	25.5	68.8	65	58.5	
6	1	64-QAM	3/4	7.9	7.5	6.8	15.9	15	13.5	33.8	31.9	28.7	77.4	73.1	65.8	
7	1	64-QAM	5/6	8.8	8.3	7.5	17.6	16.7	15	37.5	35.4	31.9	86	81.3	73.1	
8	1	256-QAM	3/4	10.6	10	9	21.2	20	18	45	42.5	38.3	103.2	97.5	87.8	
9	1	256-QAM	5/6	11.8	11.1	10	23.5	22.2	20	50	47.2	42.5	114.7	108.3	97.5	
10	1	1024-QAM	3/4	13.2	12.5	11.3	26.5	25	22.5	56.3	53.1	47.8	129	121.9	109.7	
11	1	1024-QAM	5/6	14.7	13.9	12.5	29.4	27.8	25	62.5	59	53.1	143.4	135.4	121.9	

802.11ax/ac/n Spatial Streams	1 (1x1 MU-MIMO)
Bluetooth Modulation	GFSK @ 1, 2 Mbps GFSK @ 125, 500 Kbps
Regulatory Certifications	United States (FCC) EU - Member countries of European Union (ETSI) Great Britain (UKCA) Canada (ISED) Australia/New Zealand (RCM) Japan (MIC)
2.4 GHz Frequency Bands	EU: 2.4 GHz to 2.483 GHz FCC/ISED: 2.4 GHz to 2.473 GHz UKCA: 2.4 GHz to 2.483 GHz MIC: 2.4 GHz to 2.483 GHz RCM: 2.4 GHz to 2.483 GHz
5 GHz Frequency Bands	EU 5.15 GHz to 5.35 GHz 5.47 GHz to 5.725 GHz 5.725 GHz to 5.85 GHz FCC 5.15 GHz to 5.35 GHz

Feature	Description	
	5.47 GHz to 5.725 GHz	
	5.725 GHz to 5.85 GHz	
	ISED	
	5.15 GHz to 5.35 GHz	
	5.47 GHz to 5.725 GHz	
	5.725 GHz to 5.85 GHz	
	UKCA	
	5.15 GHz to 5.35 GHz	
	5.47 GHz to 5.730 GHz	
	5.725 GHz to 5.850 GHz	
	MIC	
	5.15 GHz to 5.35 GHz	
	5.47 GHz to 5.725 GHz	
	RCM	
	5.15 GHz to 5.35 GHz	
	5.47 GHz to 5.725 GHz	
	5.725 GHz to 5.85 GHz	
Transmit Power	802.11a	
	6 Mbps	17 dBm (50.11 mW)
Note: Transmit power on each channel varies per individual country regulations. All values are nominal with +/-2 dBm tolerance at room temperature. Tolerance could be up to +/-2.5 dBm across operating temperature.	54 Mbps	16.5 dBm (44.66 mW)
	802.11b	
	1 Mbps	18 dBm (63.09 mW)
	11 Mbps	18 dBm (63.09 mW)
	802.11g	
	6 Mbps	18 dBm (63.09 mW)
	54 Mbps	17 dBm (50.11 mW)
	802.11n (2.4 GHz)	
	HT20; MCS0-4	18 dBm (63.09 mW)
	HT20; MCS5-7	16 dBm (39.81 mW)
Note: HT20/VHT20/HE20 – 20 MHz-wide channels	802.11ax (2.4 GHz)	
	HE20; MCS0-4	18 dBm (63.09 mW)
	HE20; MCS5-7	16 dBm (39.81 mW)
	HE20; MCS8-9	14 dBm (25.11 mW)
	HE20; MCS13	10.5 dBm (19.95 mW)
	802.11n (5 GHz)	
	HT20; MCS0-4	17 dBm (50.11 mW)
	HT20; MCS5-7	16.5 dBm (44.66 mW)
	802.11ac (5 GHz)	
	VHT20; MCS0-4	17 dBm (50.11 mW)
	VHT20; MCS5-7	16.5 dBm (44.66 mW)
	VHT20; MCS8	14 dBm (25.12 mW)
	802.11ax (5 GHz)	
	HE20; MCS0-4	17 dBm (50.11 mW)
	HE20; MCS5-7	16.5 dBm (44.66 mW)
	HE20; MCS8-9	14 dBm (25.12 mW)
	HE20; MC10-11	13 dBm (19.95 mW)
	Bluetooth	
	LE (1 Mbps, 2 Mbps)	7 dBm (5.01 mW) , Maximum
	LE-LR (S=2, S=8)	7 dBm (5.01 mW) , Maximum

Feature	Description
Typical Receiver Sensitivity (PER < = 10%) <i>Note: All values nominal, +/-2 dBm.</i>	802.11a:
	6 Mbps -92 dBm
	54 Mbps -75 dBm
	802.11b:
	1 Mbps -97 dBm (PER < 8%)
	11 Mbps -90 dBm (PER < 8%)
	802.11g:
	6 Mbps -94 dBm
	54 Mbps -77 dBm
	802.11n (2.4 GHz)
	6.5 Mbps (MCS0; HT20) -94 dBm
	65 Mbps (MCS7; HT20) -75 dBm
	802.11ax (2.4 GHz)
	7.3 Mbps (MCS0; HE20) -94 dBm
	121.9 Mbps (MCS11; HE20) -64 dBm
	7.3 Mbps (MCS0; HE20/RU242) -94 dBm
	802.11n (5 GHz)
	6.5 Mbps (MCS0; HT20) -92 dBm
	65 Mbps (MCS7; HT20) -73 dBm
	802.11ac (5 GHz)
	6.5 Mbps (MCS0; VHT20) -92 dBm
	78 Mbps (MCS8; VHT20) -70 dBm
	802.11ax (5 GHz)
	7.3 Mbps (MCS0; HE20) -92 dBm
	121.9 Mbps (MCS11; HE20) -61 dBm
	7.3 Mbps (MCS0; HE20/RU242) -92 dBm
	Bluetooth:
	LE-1 Mbps -96 dBm
	LE-2 Mbps -94 dBm
	LE-LR (S=2) -102 dBm
	LE-LR (S=8) -107 dBm
Operating Systems Supported	ThreadX RTOS NetX Secure TLS 1.3 NetX Duo (TCP/IP)
Security	WPA, WPA2 (Enterprise) and WPA3 (Enterprise) support for powerful encryption and authentication
Compliance	EU
	EN 300 328 EN 62368-1:2014
	EN 301 489-1 EN 300 440
	EN 301 489-17 EN 303 687
	EN 301 893 2011/65/EU (RoHS)
	FCC
	47 CFR FCC Part 15.247 RSS-247
	47 CFR FCC Part 15.407 RSS-248
	47 CFR FCC Part 2.1091
	ISED Canada
	AS/NZS
	AS/NZS 4268:2017
	MIC
	ARIB STD-T66/RCR STD-33 (2.4 GHz)
	ARIB STD-T71 (5 GHz)

Feature	Description
Certifications	<i>Bluetooth®</i> SIG Qualification 
Warranty	One Year Warranty
<i>All specifications are subject to change without notice</i>	

5 Block Diagrams

5.1 Veda IF912 module Block Diagram

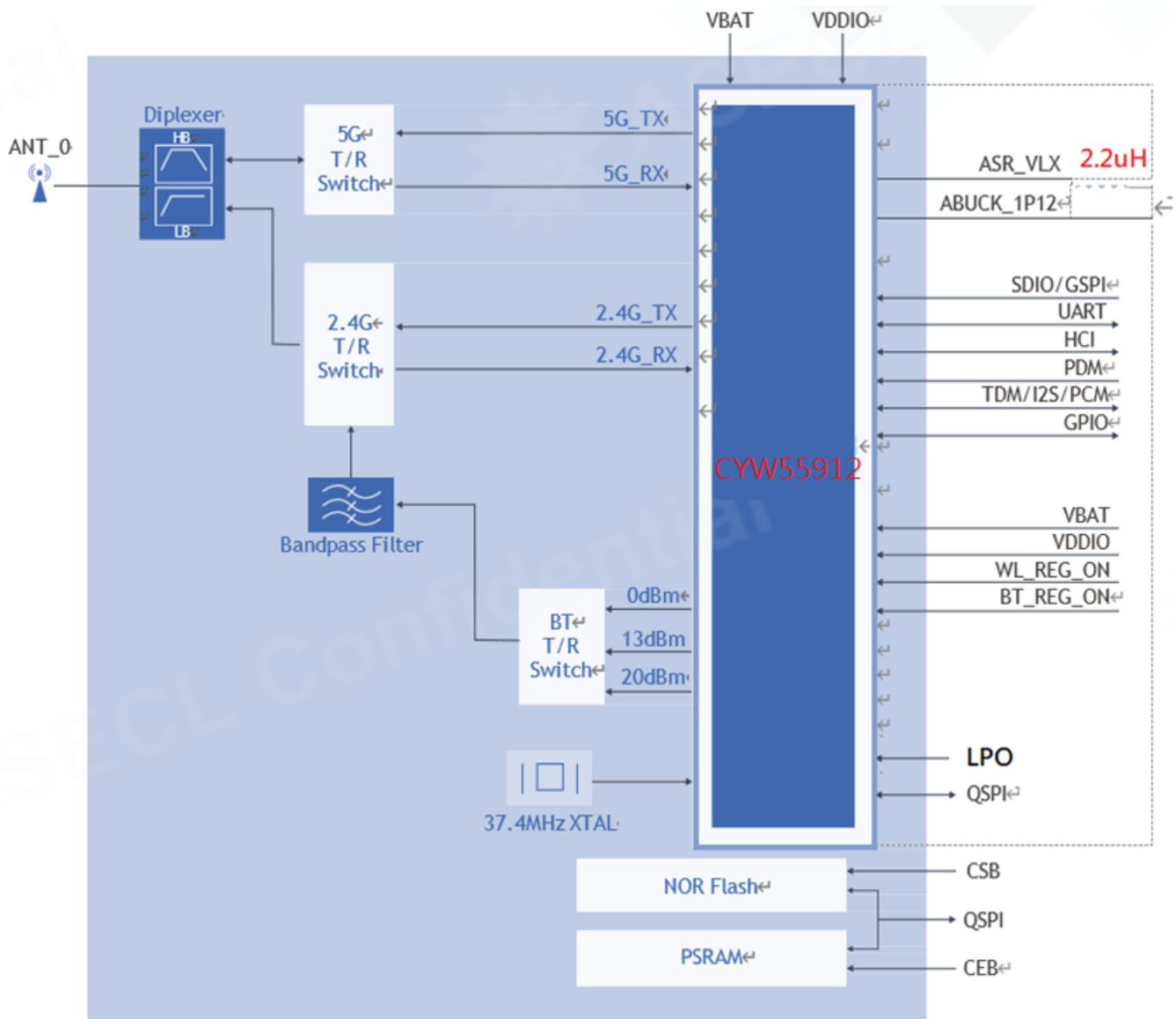


Figure 1: Veda IF912 SIP module block diagram

Note: For embedded memory variant, please connect the QSPI bus outside the SIP. See [Veda IF912 Implementation Details](#).

6 Pin Definitions

Pin #	Name	Type	Voltage Ref.	Function	If Not Used
1	GND	-	-	Ground	GND
2	TDM1_MCK	I/O	VDDIO	TDM1 Interface Master Clock / I2S Master Clock / PCM interface	NC
3	GND	-	-	Ground	GND
4	TDM1_SCK	I/O	VDDIO	TDM1 Interface Slave Clock / I2S Interface Clock / PCM interface	NC
5	GND	-	-	Ground	GND
6	TDM1_WS	I/O	VDDIO	TDM1 Interface Word Select / I2S Interface Word Select / PCM interface	NC
7	TDM1_DO	I/O	VDDIO	TDM1 Interface Data Out / I2S Interface Data Out / PCM interface	NC
8	TDM1_DI	I/O	VDDIO	TDM1 Interface Data In / I2S Interface Data In / PCM interface	NC
9	BT_DEV_WAKE	I	VDDIO	Bluetooth Device Wake-up	NC
10	WL_DEV_WAKE	I	VDDIO	WLAN Device Wake-up / Programmable General purpose I/O	NC
11	BT_HOST_WAKE	O	VDDIO	Host wake up	NC
12	GND	-	-	Ground	GND
13	DIP_OUT	RF	-	WIFI+BT RF output port 0	50 ohm terminated
14	GND	-	-	Ground	GND
15	GND	-	-	Ground	GND
16	LHL_GPIO_8	I/O	VDDIO	Miscellaneous general purpose GPIO_8	NC
17	LHL_GPIO_9	I/O	VDDIO	Miscellaneous general purpose GPIO_9	NC
18	LHL_GPIO_3	I/O	VDDIO	Miscellaneous general purpose GPIO_3	NC
19	LHL_GPIO_5	I/O	VDDIO	Miscellaneous general purpose GPIO_5	NC
20	GND	-	-	Ground	GND
21	LPO_IN	I	VDDIO	External sleep clock input (32.768 KHz) Note: Needed for Bluetooth® Low Energy to support low power mode.	-
22	GND	-	-	Ground	GND
23	WL_HOST_WAKE	O	VDDIO	WLAN HOST WAKE / Programmable General purpose I/O	NC
24	BT_UART_TXD	O	VDDIO	UART Serial Output. Serial data output for the HCI UART interface.	NC
25	GND	-	-	Ground	GND
26	ABUCK_1P12	PWR input	-	Normal 1.12V power input and 0.74V when in sleep mode. Please connect to the filtered ABUCK voltage. See pin-33 and pin-34.	-
27	ABUCK_1P12	PWR input	-	See Veda IF912 Implementation Details .	-
28	GND	-	-	Ground	GND
29	TDM2_MCK	I/O	VDDIO	TDM2 Interface Master Clock / I2S Master Clock/ PCM interface	NC
30	GND	-	-	Ground	GND
31	TDM2_SCK	I/O	VDDIO	TDM2 Interface Slave Clock / I2S Interface Clock / PCM interface	NC
32	GND	-	-	Ground	GND

Pin #	Name	Type	Voltage Ref.	Function	If Not Used
33	ASR_VLX	PWR output	-	Analog Switching Regulator (ABUCK) power stage output. Please connect to external L-C Filter (2.2uH+ 4.7uF) and connected to ABUCK_1P12 (pin-26; pin-27)	-
34	ASR_VLX	PWR output	-	See Veda IF912 Implementation Details	-
35	GND	-	-	Ground	GND
36	GND	-	-	Ground	GND
37	VBAT	PWR	3.3V	Main DC supply voltage for module. Operational: VBAT is 3.0V to 4.8V	-
38	VBAT	PWR	3.3V	- VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds. - VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.	-
39	GND	-	-	Ground	GND
40	SDIO_CLK	I	VDDIO	SDIO Clock Input / gSPI Clock Interface	NC
41	GND	-	-	Ground	GND
42	SDIO_CMD	I/O	VDDIO	SDIO Command Line/ gSPI MOSI Interface	NC
43	SDIO_DATA_0	I/O	VDDIO	SDIO Data line 0/ gSPI MISO Interface	NC
44	SDIO_DATA_1	I/O	VDDIO	SDIO Data line 1/ gSPI interrupt Interface	NC
45	SDIO_DATA_2	I/O	VDDIO	SDIO Data line 2/ gSPI Interface This pin is also used for strapping option for SDIO or gSPI. Default pull during strapping="H" for SDIO bus; pull it "L" during strapping for gSPI bus.	NC
46	SDIO_DATA_3	I/O	VDDIO	SDIO Data line 3/ gSPICS Interface	NC
47	GND	-	-	Ground	GND
48	SCLK	I/O	VDDIO	Serial Clock input for embedded memory. For No embedded memory variant, keep this pin NC.	NC
49	GND	-	-	Ground	GND
50	SI	I/O	VDDIO	Serial Data Input / Serial Data Input Output 0 for embedded memory. For No embedded memory variant, keep this pin NC.	NC
51	SIO2	I/O	VDDIO	Serial Data Input / Serial Data Input Output 2 for embedded memory. For No embedded memory variant, keep this pin NC.	NC
52	SIO1	I/O	VDDIO	Serial Data Input / Serial Data Input Output 1 for embedded memory. For No embedded memory variant, keep this pin NC.	NC
53	HOLDB	I/O	VDDIO	Hold Input/Serial Data Input Output 3 for embedded memory. For No embedded memory variant, keep this pin NC.	NC
54	CEB	I	VDDIO	Chip Select input, active low (CE pin for embedded PSRAM) For No embedded memory variant, keep this pin NC.	NC
55	CSB	I	VDDIO	Chip Select input, active low (CS pin for embedded NOR Flash) For No embedded memory variant, keep this pin NC.	NC

Pin #	Name	Type	Voltage Ref.	Function	If Not Used
56	SMIF_SPHB_DQ0	I/O	VDDIO	SMIF data line 0. - Connect to external NOR Flash IO0 and external PSRAM SIO[0]. - Connect to SI (pin-50) for embedded Memory variant.	NC
57	SMIF_SPHB_DQ1	I/O	VDDIO	SMIF data line 1. - Connect to external NOR Flash IO1 and external PSRAM SIO[1]. - Connect to SIO1 (pin-52) for embedded Memory variant.	NC
58	GND	-	-	Ground	GND
59	VDDIO	PWR input	-	1.8 V IO supply for WLAN GPIOs VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.	NC
60	BT_GPIO_0	I/O	VDDIO	Bluetooth® general purpose I/O	NC
61	BT_GPIO_7	I/O	VDDIO	Bluetooth® general purpose I/O	NC
62	BT_GPIO_16	I/O	VDDIO	Bluetooth® general purpose I/O	NC
63	BT_GPIO_17	I/O	VDDIO	Bluetooth® general purpose I/O	NC
64	BT_GPIO_5	I/O	VDDIO	Bluetooth® general purpose I/O	NC
65	BT_GPIO_6	I/O	VDDIO	Bluetooth® general purpose I/O	NC
66	BT_GPIO_3	I/O	VDDIO	Bluetooth® general purpose I/O	NC
67	BT_GPIO_4	I/O	VDDIO	Bluetooth® general purpose I/O	NC
68	BT_GPIO_2	I/O	VDDIO	Bluetooth® general purpose I/O	NC
69	GND	-	-	Ground	GND
70	DMIC_DATA	I/O	VDDIO	Digital mic data	NC
71	GND	-	-	Ground	GND
72	LHL_GPIO_4	I/O	VDDIO	Miscellaneous general purpose GPIO_4	NC
73	LHL_GPIO_2	I/O	VDDIO	Miscellaneous general purpose GPIO_2	NC
74	LHL_GPIO_6	I/O	VDDIO	Miscellaneous general purpose GPIO_6	NC
75	GND	-	-	Ground	GND
76	GND	-	-	Ground	GND
77	MIC_P	I	VDDIO	ADC microphone positive input	NC
78	GND	-	-	Ground	GND
79	BT_UART_RXD	I	VDDIO	UART Serial Input. Serial data input for the HCI UART interface.	NC
80	BT_UART_RTS_N	O	VDDIO	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. Bluetooth® LED control pin.	NC
81	BT_UART_CTS_N	I	VDDIO	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.	NC
82	BT_REG_ON	I	VDDIO	Used by the PMU to power up or power down the internal regulators used by the Bluetooth® section. When deasserted, this pin holds the Bluetooth® section in reset. This pin has an internal 50 kΩ pull-down resistor by default. that is auto enabled/disabled by programming.	-
83	WL_REG_ON	I	VDDIO	Not used for IF913/IF912. This should be tied to GND on board.	GND

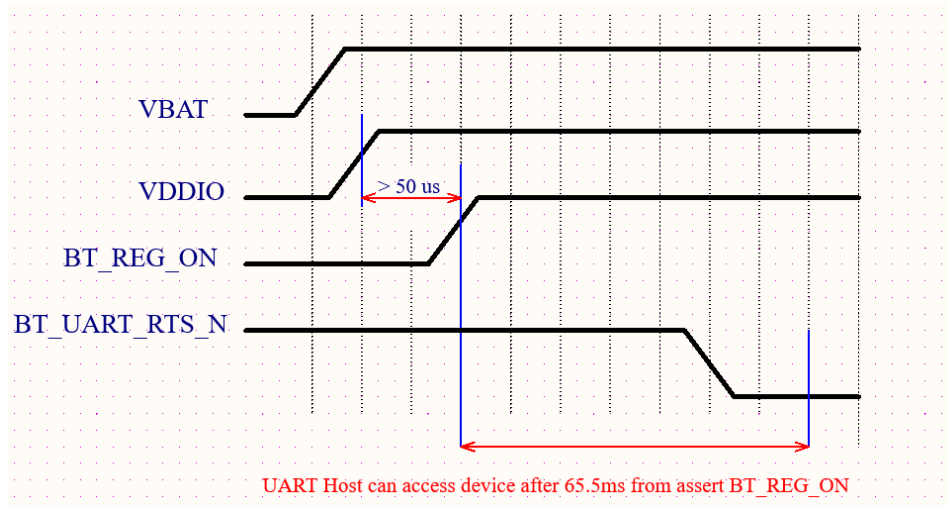
Pin #	Name	Type	Voltage Ref.	Function	If Not Used
84~86	GND	-	-	Ground	GND
87	TDM2_DI	I/O	VDDIO	TDM2 Interface Data In / I2S Interface Data In / PCM interface	NC
88	TDM2_DO	I/O	VDDIO	TDM2 Interface Data Out / I2S Interface Data Out / PCM interface	NC
89	TDM2_WS	I/O	VDDIO	TDM2 Interface Word Select / I2S Interface Word Select / PCM interface	NC
90	VCC	PWR	-	Memory 1.8V power supply	-
91	GND	-	-	Ground	GND
92	SMIF_SPHB_CLK	O	VDDIO	SMIF clock output - Connect to external NOR Flash SCK and external PSRAM SCK. - Connect to SCK (pin-48) for embedded Memory variant.	GND
93	GND	-	-	Ground	GND
94	SMIF_SPHB_DQ2	I/O	VDDIO	SMIF data line 2. - Connect to external NOR Flash IO2 and external PSRAM SIO[2]. - Connect to SIO2 (pin-51) for embedded Memory variant.	-
95	SMIF_SPHB_DQ3	I/O	VDDIO	SMIF data line 3. - Connect to external NOR Flash IO3 and external PSRAM SIO[3]. - Connect to HOLD (pin-53) for embedded Memory variant.	NC
96	SMIF_SPHB_CS0_N	O	VDDIO	SMIF chip select0 active-low output - Connect to external NOR Flash CS# pin. - Connect to CSB (pin-55) for embedded Memory variant.	NC
97	SMIF_SPHB_CS1_N	O	VDDIO	SMIF chip select1 active-low output - Connect to external PSRAM CE# pin. - Connect to CEB (pin-54) for embedded Memory variant.	NC
98~107	GND	-	-	Ground	GND
E1~E4	GND	-	-	Ground	GND

7 Veda IF912 Implementation Details

7.1 Power up sequency timing

To maintain stable MCU and Bluetooth starting up, below power up sequency timing is required.

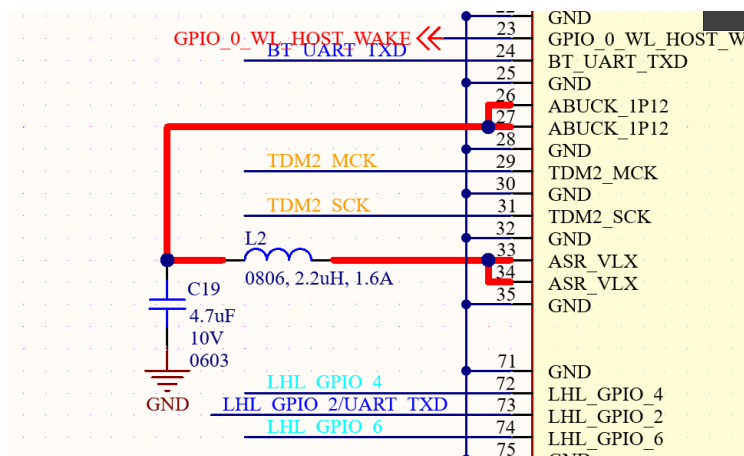
- VBAT and VDDIO should not rise 10%-90% faster than 40 microseconds.
- VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.



7.2 L-C filter for Buck switching regulator

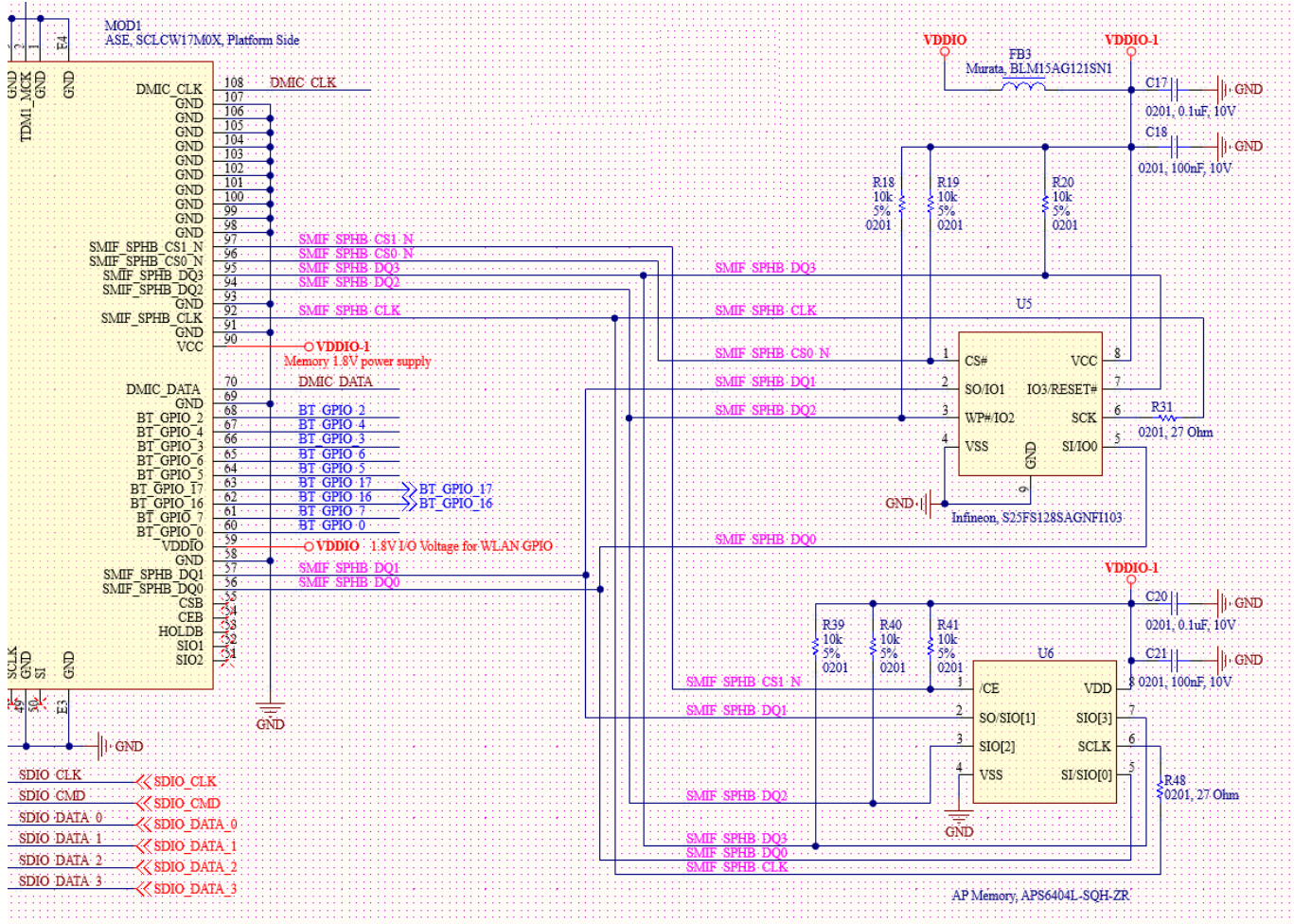
An Analog Switching Regulator (ASR or ABUCK) is built in the Veda IF912 module, the ABUCK output is brought out to pin-33 and pin-34. A L-C filter (2.2uH and 4.7uF) is required to filter out the switching noise before it feeds into ABUCK_1P12 (pin-26 and pin-27). Keep the 2.2uH and 4.7uF as close to Veda IF913 as possible to keep the current flow loop small as you can. Please refer to the Ezurio DVK for the detail placement and routing. Detail parts information is shown in below.

- 2.2uH: 74479276222C (Wurth Elektronik)
- 4.7uF: GRM188C71A475KE11# (Murata)



7.3 Serial Memory Interface (SMIF) Connection.

- For the Veda IF912 without embedded memory variant (453-00396R), user can add external memory (NOR Flash and PSRAM) to the SMIF. Example connections are shown below. **Note: VDDIO is limited to 1.8V.**



-
- The diagram illustrates the pin connections for the MOD1 ASE, SCLCW17M0X, Platform Side. It shows two main connector blocks, E4 and E3, and their corresponding internal pin connections to various components.
- Connector E4 (Top Left):**
- Pin 4: TDM1_SCK
 - Pin 3: GND
 - Pin 2: TDM1_MCK
 - Pin 1: GND
 - Pin E4: GND
- Connector E3 (Bottom Left):**
- Pin 4: GND
 - Pin 48: SCLK
 - Pin 49: GND
 - Pin 50: SI
 - Pin E3: GND
- Internal Pin Connections (Right Side):**
- DMIC_CLK:** Pins 108 to 90 (GND).
 - DMIC_DATA:** Pins 70 to 60 (GND).
 - BT GPIO:** Pins 68 to 60 (GND).
 - SMIF_SPHB:** Pins 97 to 90 (GND).
 - SMIF_SPHB_CS1_N:** Pin 96.
 - SMIF_SPHB_CS0_N:** Pin 95.
 - SMIF_SPHB_DQ3:** Pin 94.
 - SMIF_SPHB_DQ2:** Pin 93.
 - SMIF_SPHB_CLK:** Pin 92.
 - SMIF_SPHB_DQ1:** Pin 57.
 - SMIF_SPHB_DQ0:** Pin 56.
 - SMIF_SPHB_CS0_N:** Pin 55.
 - SMIF_SPHB_CS1_N:** Pin 54.
 - SMIF_SPHB_DQ3:** Pin 53.
 - SMIF_SPHB_DQ1:** Pin 52.
 - SMIF_SPHB_DQ2:** Pin 51.
- Power and Ground Connections:**
- VCC:** Pin 90.
 - GND:** Pins 98, 97, 96, 95, 94, 93, 92, 91, 90, 69, 68, 67, 66, 65, 64, 63, 62, 61, 60, 59, 58, 57, 56, 55, 54, 53, 52, 51.
 - DMIC_CLK:** Pin 108.
 - DMIC_DATA:** Pin 70.
 - BT_GPIO_2:** Pin 68.
 - BT_GPIO_4:** Pin 67.
 - BT_GPIO_3:** Pin 66.
 - BT_GPIO_6:** Pin 65.
 - BT_GPIO_5:** Pin 64.
 - BT_GPIO_17:** Pin 63.
 - BT_GPIO_16:** Pin 62.
 - BT_GPIO_7:** Pin 61.
 - BT_GPIO_0:** Pin 60.
 - SMIF_SPHB_CS1_N:** Pin 97.
 - SMIF_SPHB_CS0_N:** Pin 96.
 - SMIF_SPHB_DQ3:** Pin 94.
 - SMIF_SPHB_DQ2:** Pin 93.
 - SMIF_SPHB_CLK:** Pin 92.
 - SMIF_SPHB_DQ1:** Pin 57.
 - SMIF_SPHB_DQ0:** Pin 56.
 - SMIF_SPHB_CS0_N:** Pin 55.
 - SMIF_SPHB_CS1_N:** Pin 54.
 - SMIF_SPHB_DQ3:** Pin 53.
 - SMIF_SPHB_DQ1:** Pin 52.
 - SMIF_SPHB_DQ2:** Pin 51.
- Power and Ground Connections (Bottom):**
- VCC:** Pin 90.
 - GND:** Pins 98, 97, 96, 95, 94, 93, 92, 91, 90, 69, 68, 67, 66, 65, 64, 63, 62, 61, 60, 59, 58, 57, 56, 55, 54, 53, 52, 51.
 - DMIC_CLK:** Pin 108.
 - DMIC_DATA:** Pin 70.
 - BT_GPIO_2:** Pin 68.
 - BT_GPIO_4:** Pin 67.
 - BT_GPIO_3:** Pin 66.
 - BT_GPIO_6:** Pin 65.
 - BT_GPIO_5:** Pin 64.
 - BT_GPIO_17:** Pin 63.
 - BT_GPIO_16:** Pin 62.
 - BT_GPIO_7:** Pin 61.
 - BT_GPIO_0:** Pin 60.
 - SMIF_SPHB_CS1_N:** Pin 97.
 - SMIF_SPHB_CS0_N:** Pin 96.
 - SMIF_SPHB_DQ3:** Pin 94.
 - SMIF_SPHB_DQ2:** Pin 93.
 - SMIF_SPHB_CLK:** Pin 92.
 - SMIF_SPHB_DQ1:** Pin 57.
 - SMIF_SPHB_DQ0:** Pin 56.
 - SMIF_SPHB_CS0_N:** Pin 55.
 - SMIF_SPHB_CS1_N:** Pin 54.
 - SMIF_SPHB_DQ3:** Pin 53.
 - SMIF_SPHB_DQ1:** Pin 52.
 - SMIF_SPHB_DQ2:** Pin 51.

7.4 SDIO and gSPI strapping configuration

SDIO and gSPI in Veda IF912 are muxed together on the same pin out, please reference the pin definition table.

A strapping option pin **SDIO_DATA[2]** is used to configure between SDIO and gSPI. Default is in "H" state which is SDIO mode. Pull this pin to "L" will be set in gSPI mode.

7.4.1 SDIO mode

Veda IF912 provide support for SDIO V 3.0, including the new UHS-I modes:

- DS: Default speed (DS) up to 25 MHz, including 1 and 4-bit modes **(1.8 V signaling)**
- HS: High-speed up to 50 MHz **(1.8 V signaling)**
- SDR12: SDR up to 25 MHz (1.8 V signaling)
- SDR25: SDR up to 50 MHz (1.8 V signaling)
- SDR50: SDR up to 100 MHz (1.8 V signaling)
- DDR50: DDR up to 50 MHz (1.8 V signaling)

Notes: 1. The UHS-1 rate SDR104, that is part of the SDIO V 3.0 specification, is not supported.

2. Veda IF912 is backward compatible with SDIO V 2.0 host interfaces. Note however that it can only support 1.8 V signaling. It cannot support 3.3 V signaling during initialization post power cycle and in default/high speed SDIO V 2.0 modes. The host must use 1.8 V signaling.

According to the SDIO specification, pull-ups in the 10 kΩ to 100 kΩ range are required on the four DATA lines and the CMD line. This requirement must be met during all operating states either through the use of external pull-up resistors or through proper programming of the SDIO host's internal pull-ups.

7.4.2 gSPI mode

Veda IF912 has the option of using the simplified generic SPI (gSPI) interface/protocol.

Characteristics of the gSPI mode include:

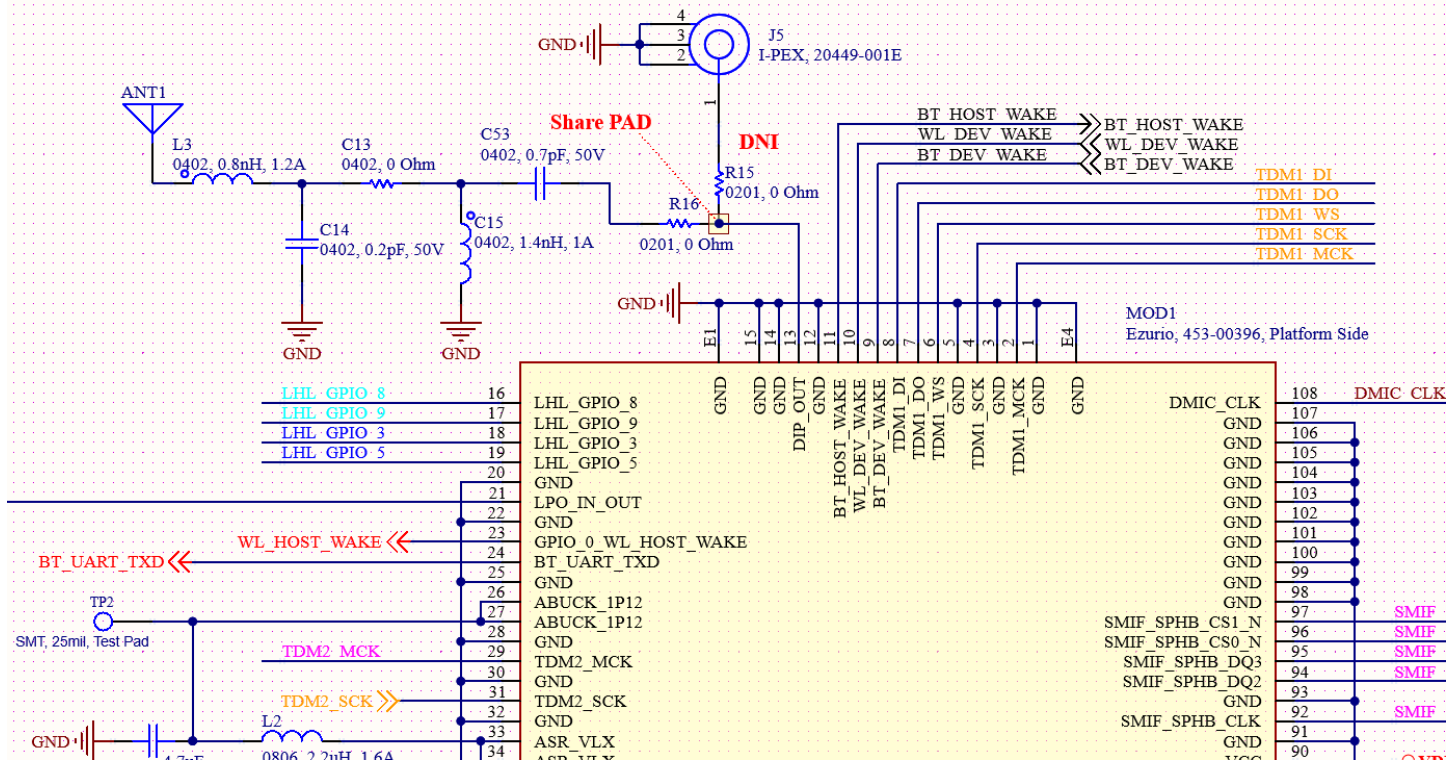
- Up to 50-MHz operation
- Fixed delays for responses and data from the device
- Alignment to host gSPI frames (16 or 32 bits)
- Up to 2-KB frame size per transfer
- Little-endian and big-endian configurations
- A configurable active edge for shifting
- Packet transfer for CCM/CP Traffic/Data Exchange

Note: gSPI mode is enabled using the strapping option pins.

7.5 MHF4 and Embedded PCB antenna

The Veda IF912 DVK design has two antenna connection options which are MHF4 and embedded PCB antenna. Pop on R15, users can get the RF signal out at MHF4 connector for external antenna. Pop on R16 will allow users to use the embedded PCB antenna.

Please copy the components' location for the RF trace from the DVK to maintain the RF performance and adopt Ezurio certification grant.



8 Mechanical Specifications

Veda IF912 SIP package is 11 x 7 x 1.4 mm. Detailed drawings are shown in

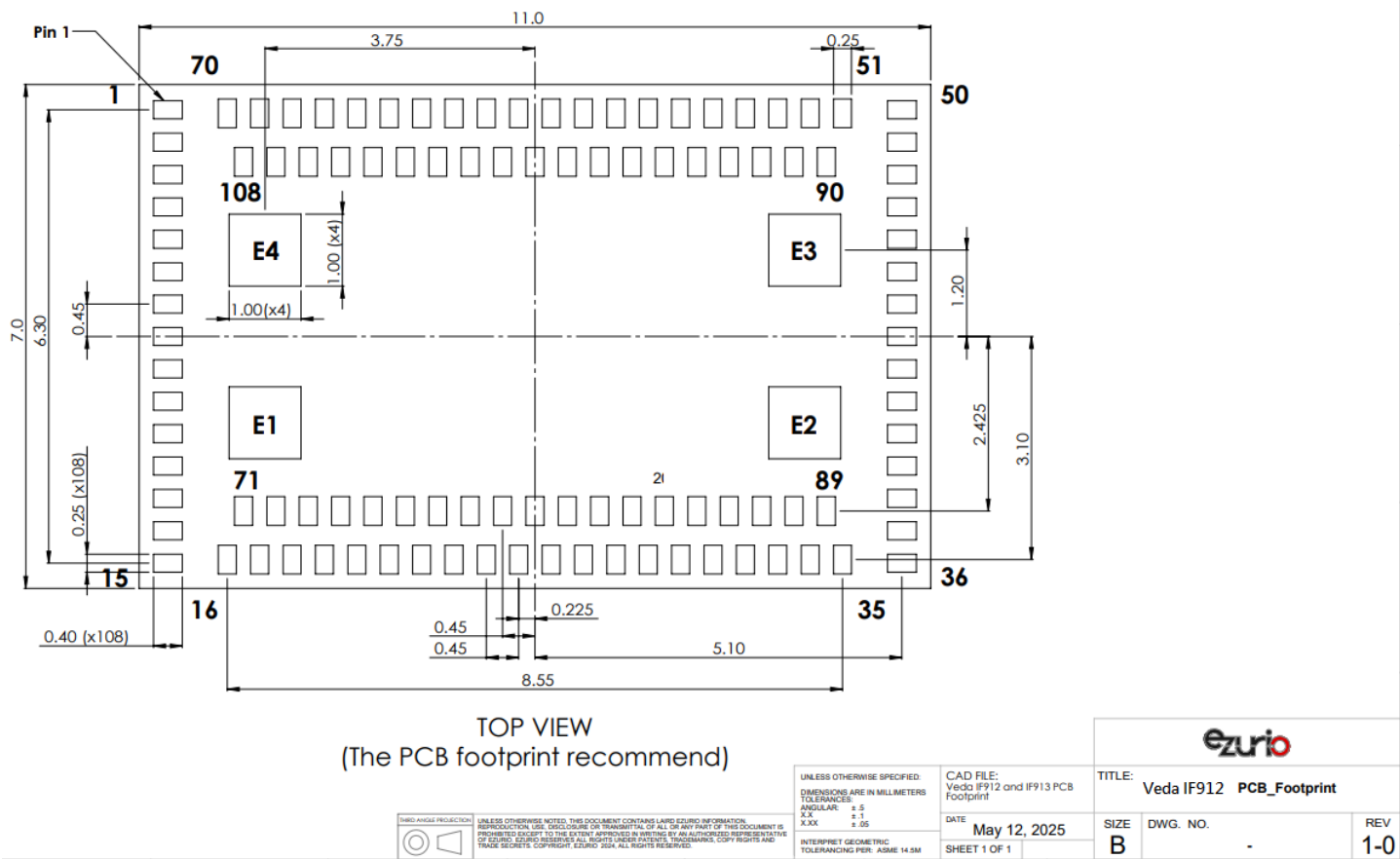


Figure 2.



		
TITLE: Veda IF912 PCB_Footprint		
SIZE B	DWG. NO. -	REV 1-0

Note: Dimensions are in millimeters tolerances:

Angular:	± 0.5
X.X:	± 0.1
X.XX:	± 0.05

9 Material handling information

9.1 Required Storage Conditions

9.1.1 Prior to Opening the Dry Packing

The following are required storage conditions *prior to opening the dry packing*:

- Normal temperature: 5~40 °C
- Normal humidity: 80% (Relative humidity) or less
- Storage period: One year or less

Note: Humidity means relative humidity.

9.1.2 After Opening the Dry Packing

The following are required storage conditions *after opening the dry packing* (to prevent moisture absorption):

- Storage conditions for one-time soldering:
 - Temperature: 5-25°C
 - Humidity: 60% or less
 - Period: 72 hours or less after opening
- Storage conditions for two-time soldering
 - Storage conditions following opening and prior to performing the 1st reflow:
 - Temperature: 5-25°C
 - Humidity: 60% or less
 - Period: A hours or less after opening
 - Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow
 - Temperature: 5-25°C
 - Humidity: 60% or less
 - Period: B hours or less after completion of the 1st reflow

Note: Should keep A+B within 72 hours.

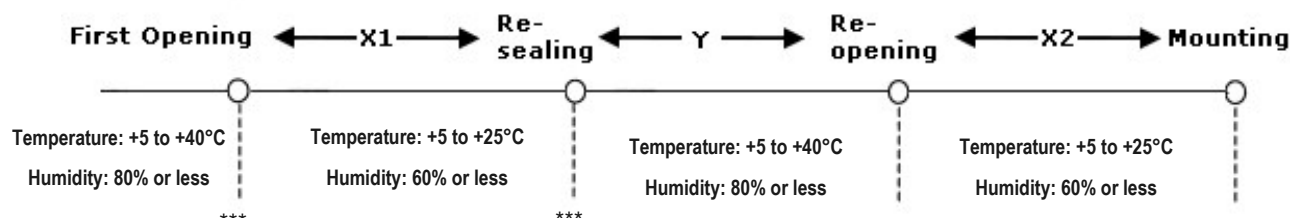
9.1.3 Temporary Storage Requirements after Opening

The following are temporary storage requirements after opening:

- Only re-store the devices once prior to soldering.
- Use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using vacuumed heat-sealing.

The following indicate the required storage period, temperature, and humidity for this temporary storage:

- Storage temperature and humidity:



- Storage period:
 - X1+X2 – Refer to **Material handling information**
 - Required Storage Conditions. Keep is X1+X2 within 72 hours.

- Y – Keep within two weeks or less.

9.2 Baking Conditions

Baking conditions and processes for the module follow the J-STD-033 standard which includes the following:

- The calculated shelf life in a sealed bag is 12 months at < 40°C and < 80% relative humidity.
- Once the packaging is opened, the SiP must be mounted (per **MSL4/Moisture Sensitivity Level 4**) within 72 hours at < 30 °C and < 60% relative humidity.

If the SiP is not mounted within 72 hours or if, when the dry pack is opened, the humidity indicator card displays >10% humidity, then the product must be baked for 48 hours at 125 °C (±5 °C).

10 Surface Mount Conditions

The following soldering conditions are recommended to ensure device quality.

10.1 Recommended Stencil Aperture

TBD

Figure 3: Veda IF912 SIP stencil aperture

Note: The stencil thickness is 0.12mm.

10.2 Soldering profile

Note: When soldering, the stencil thickness should be 0.12 mm.

Convection reflow or IR/Convection reflow (one-time soldering or two-time soldering in air or nitrogen environment)

Measuring point – IC package surface

Temperature profile:

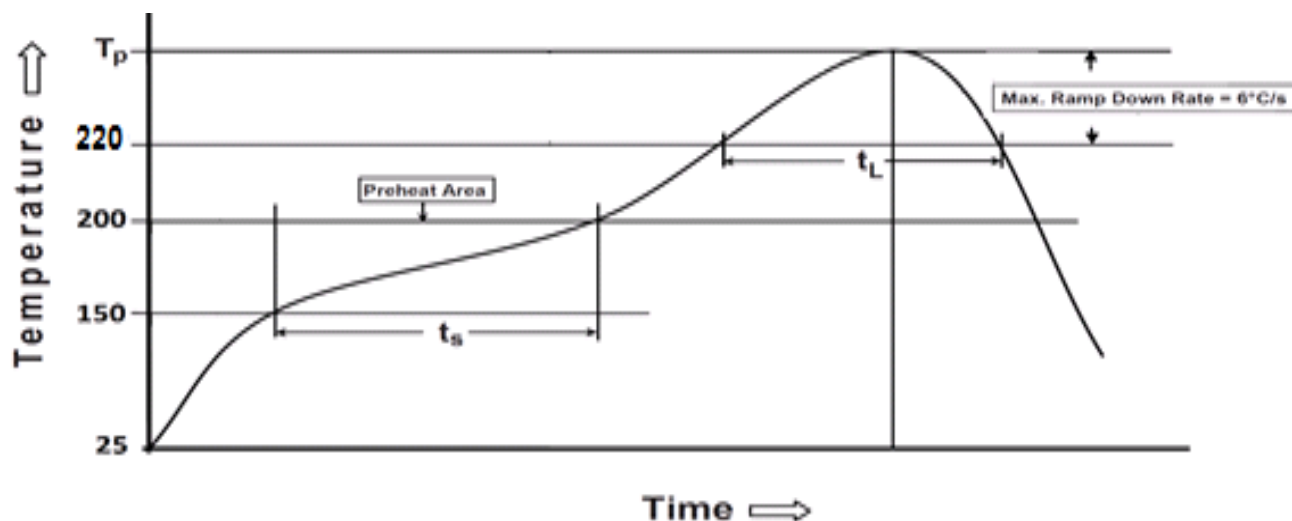


Figure 4: Temperature profile

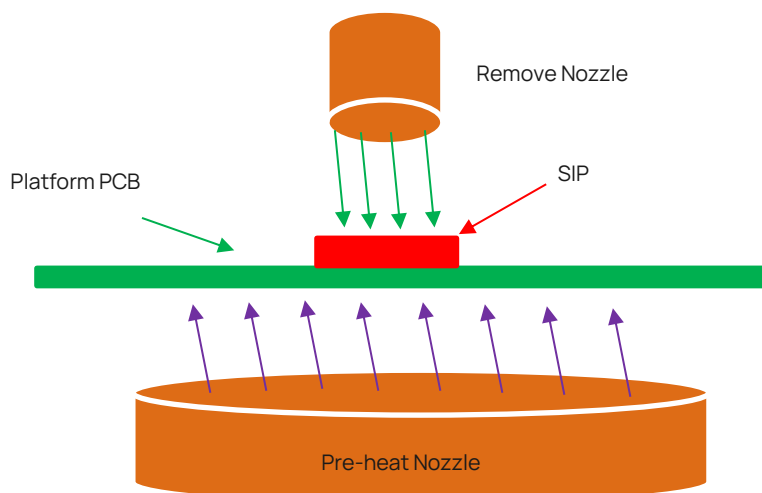
- Solder paste alloy: SAC305 (Sn96.5 / Ag3.0 / Cu 0.5)
- Pre-heat temperature: 150°C ~ 200°C; Soak time: 60 second ~ 120 second
- Peak temperature: 235°C ~ 250°C
- Time above 220°C: 40 second ~ 90 second
- Optimal cooling rate < 3°C/second
- The oxygen concentration < 2000 ppm

11 Cautions When Removing the SIP from the Platform for RMA

- Bake the platform PCBA before removing the Veda IF912 module from the platform.
- Remove the Veda IF912 module by using a hot air gun. This process should be carried out by a skilled technician.

Recommended conditions:

- One-side component platform:
 - Set the hot plate at 280°C.
 - Put the platform on the hot plate for 8~10 seconds.
 - Remove the device from platform.
- Two-side components platform:
 - Use two hot air guns.
 - On the bottom, use a pre-heated nozzle (temp setting of 200~250°C) at a suitable distance from the platform PCB.
 - On the top, apply a remove nozzle (temp setting of 330°C). Heat until device can be removed from platform PCB.

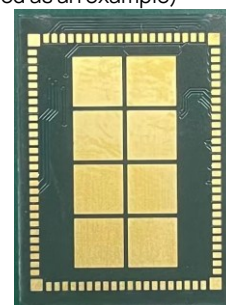


- Remove the residue solder under the bottom side of device. (Note: Alternate module pictured as an example)



(Not accepted for RMA)

Figure 5: Example module with residue solder on the bottom



(Accepted for RMA analysis)

Figure 6: module without residue solder

- Remove and clean the residue flux as needed.

11.1.1 Precautions for Use

- Opening/handling/removing must be done on an anti-ESD treated workbench. All workers must also have undergone anti-ESD treatment.
- The devices should be mounted within one year of the date of delivery.
- The Veda IF912 modules are MSL level 4 rated.

12 Certified Antennas

The Veda IF912 module was tested with antennas listed in the following table. The OEM can choose a different manufacturer's antenna but must make sure it is of same type and that the gain is less than or equal to the antenna that is approved for use.

Manufacturer	Model	Ezurio Part Number	Type	Connector	Peak Gain (dBi)		
					2.4GHz	5GHz	6GHz
Ezurio (formerly Laird Connectivity)	FlexMIMO 6E	EFD2471A3S-10MH4L	PIFA	MHF4L	2.2	3.8	3.3
Ezurio (formerly Laird Connectivity)	FlexPIFA 6E	EFB2471A3S-10MH4L	PIFA	MHF4L	2.2	3.9	3.8
Ezurio (formerly Laird Connectivity)	Mini NanoBlade Flex 6 GHz	EMF2471A3S-10MH4L	PCB Dipole	MHF4L	2.4	4.4	5.2
Joymax Electronics	Dipole 6E	TWX-100BRSAX-2001 / TWX-100BRS3B	Dipole	RP-SMA	2	4.0	4.0

13 Additional Information

Please contact your local sales representative or our support team for further assistance:

Headquarters	Ezurio 50 S. Main St. Suite 1100 Akron, OH 44308 USA
Website	www.ezurio.com/
Technical Support	www.ezurio.com/resources/support
Sales Contact	www.ezurio.com/contact

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