UD info Corp.

Industrial M.2 2280 PCIe SSD
M2P-80UB Series
Product DataSheet

UD info CORP.

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Revision History

Revision	Draft Date	History	Author
1.0	2018/7/19	New release	Golden Lee
1.1	2018/11/9	Update Capacity	Golden Lee
1.2	2019/5/3	Update Capacity and Performance	Golden Lee
1.3	2019/5/22	Removed E12C information	Golden Lee

Product Overview

- **Capacity**
  - 120/128GB up to 1920GB/2TB
- **Form Factor**
  - E12 M.2 2280-S2-M (BGA272 x2)
  - E12 M.2 2280-D2-M (BGA132/152 x4)
- **PCIe Interface**
  - NVMe PCIe Gen3 x4
- **Compliance**
  - NVMe 1.3
  - PCI Express Base 3.1
- **Flash Interface**
  - Transfer rate up to 533Mbps
  - Up to 2pcs of BGA272 flash
  - Up to 4pcs of BGA132/152 flash
- **Performance** [Note1]
  - Read up to 3,400 MB/s
  - Write up to 3,000 MB/s
- **Power Consumption** [Note2]
  - Idle mode: < 910mW
  - L1.2 < 2mW
- **Power Management**
  - Support APST
  - Support ASPM
  - Support L1.2
- **Advanced Flash Management**
  - Static and Dynamic Wear Leveling
  - Bad Block Management
  - TRIM
  - SMART
  - Over-Provision
- **Reliability**
  - MTBF more than 1,800,000 hours
  - Uncorrectable Bit Error Rate(UBER) < 1 sector per 10^{16} bits read
- **Temperature Range** [Note4]
  - Operation (Standard): 0°C ~ 70°C
  - Storage: -40°C ~ 85°C
  - Operation airflow: 800LFM at 35°C ambient
- **Compliant**
  - RoHS
- **Features Support List**
  - End to end data path protection
  - Thermal throttling
  - SmartECC™
  - SmartRefresh™
  - Drive log
  - Support of TCG OPAL [Note3]
  - Support of TCG Pyrite [Note3]

Notes:

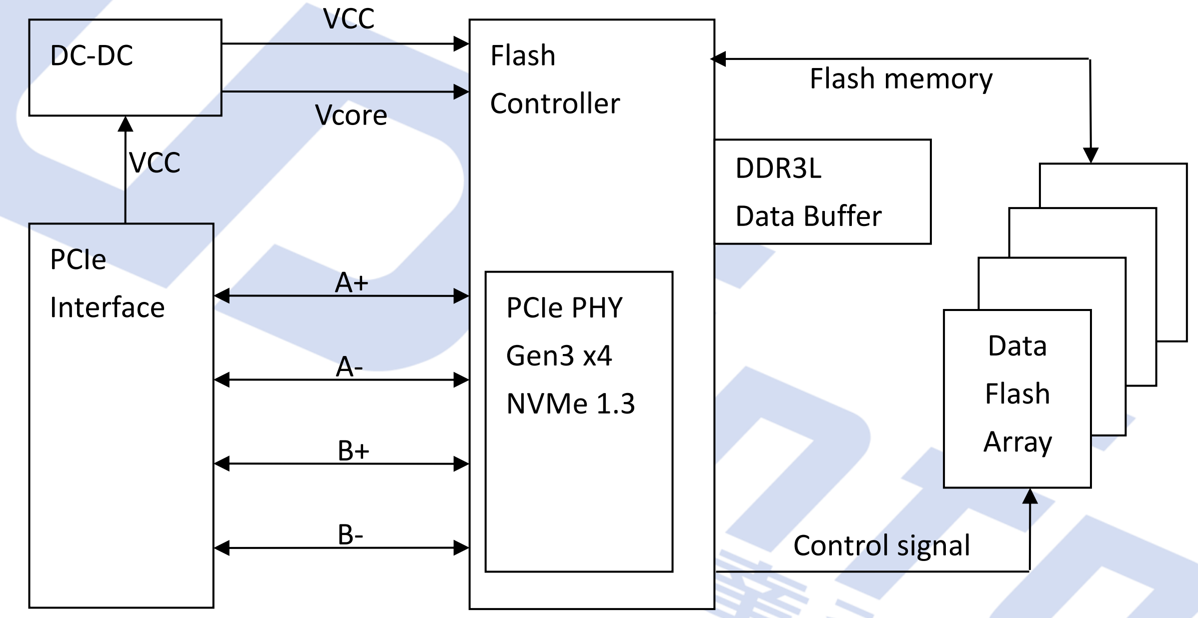
1. Refer to Chapter 2 for more details.
2. Refer to Chapter 4, section 4.2 power consumption for more details.
3. Support by a separate firmware version. Further information available upon request.
4. Operation temperature is measured by device temperature sensor.

1. INTRODUCTION

1.1. General Description

UDinfo's M.2 2280 PCIe solid state Drive delivers all the advantages of flash disk technology with PCIe Gen3 x4 interface and is fully compliant with the standard Next Generation Form Factor (NGFF) called M.2 Card Format. The M.2 2280 could provide a wide range capacity up to 1920GB and its performance can reach up to 3,400MB/s read and 3,000MB/s write based on Toshiba's BiCS3 TLC NAND flash with the choice of 256MB/512MB/1GB/2GB DDR3L. Moreover, the power consumption of the M.2 2280 is much lower than traditional hard drives, making it the best embedded solution for new platforms.

1.2. Block Diagram



M.2 2280 PCIe SSD Block Diagram

2. PRODUCT SPECIFICATIONS

- **Capacity**
  - 120/128GB up to 1920GB/2TB
- **Electrical/Physical Interface**
  - PCI Express Base Ver 3.1
  - Compliant with NVMe 1.3
  - PCIe Gen3 x 4 lane & backward compatible to PCIe Gen2 and Gen1
  - 8 IO queues supported(1 admin queue and 8 IO queue). Each IO queue support 256 entries.
  - Support power management
- **Supported NAND Flash**
  - Support Toshiba BiCS3 TLC
  - Support up to 2pcs of BGA272 flash (M.2 2280-S2)
  - Support up to 4pcs of BGA132/152 flash (M.2 2280-D2)
- **ECC Scheme**
  - Applies LDPC of ECC algorithm
- **Sector Size Support**
  - 512Bytes
  - 4KB
- **UART / GPIO**
- **Support SMART and TRIM commands**

- **LBA Range**
  - IDEMA standard

Capacity	Total Sectors (LBA)	User Data Size
120GB	234,441,648	Depended on file management
128GB	250,069,680	
240GB	468,862,128	
256GB	500,118,192	
480GB	937,703,088	
512GB	1,000,215,216	
960GB	1,875,385,008	
1TB	2,000,409,264	
1920GB	3,750,748,848	
2TB	4,000,797,360	

- **TBW (Terabytes Written)**
  - **BiCS3 TLC**

Capacity	Flash Structure	Flash Type	TBW
128GB	64GB x 2	BGA, BiCS3 TLC, 256Gb DDP	203
256GB	128GB x 2	BGA, BiCS3 TLC, 256Gb QDP	437
512GB	256GB x 2	BGA, BiCS3 TLC, 256Gb ODP	918
1024GB	256GB x 4	BGA, BiCS3 TLC, 256Gb ODP	1,856
2048GB	512GB x 4	BGA, BiCS3 TLC, 512Gb ODP	3,566

Notes:

1. Samples were built using Toshiba BiCS3 TLC NAND flash.
2. The test followed JEDEC219A client endurance workload.
3. TBW may differ according to flash configuration and platform.
4. The endurance of SSD could be estimated based on user behavior, NAND endurance cycles, and write amplification factor. It is not guaranteed by flash vendor.

- **Performance**

  - **BiCS3 TLC**

Capacity	Flash Structure	Flash Type	Sequential		Random	
			Read (MB/s)	Write (MB/s)	Read (IOPS)	Write (IOPS)
240/256GB	64GB x 4	TSB Bics3, BGA132	3,095	1,045	180K	255K
	128GB x 2	TSB Bics3, BGA272	3,100	1,050	181K	256K
480/512GB	128GB x 4	TSB Bics3, BGA132	3,400	2,100	358K	457K
	256GB x 2	TSB Bics3, BGA272	3,400	2,100	357K	456K
960GB/1TB	256GB x 4	TSB Bics3, BGA132	3,390	3,000	587K	458K
1920GB/2TB	512GB x 4	TSB Bics3, BGA152	3,390	3,000	491K	470K

Notes:

1. The performance was estimated based on Toshiba BiCS3 TLC NAND flash.
2. Performance may differ according to flash configuration and platform.
3. The table above is for reference only. Any criteria for accepting goods shall be discussed based on different flash configurations.
4. Performance is measured with the follow conditions
   (a) CrystalDiskMark 5.1.2, 1GB range, QD=32, Thread=1
   (b) IOMeter, 8GB range, 4K data size, QD=32

3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

3.1.1. Temperature and Humidity

- **High Temperature Test Condition**

	Temperature	Humidity
Operation	70°C	0% RH
Storage	85°C	0% RH

- **Low Temperature Test Condition**

	Temperature	Humidity
Operation	0°C	0% RH
Storage	-40°C	0% RH

- **High Humidity Test Condition**

	Temperature	Humidity
Operation	40°C	90% RH
Storage	40°C	93% RH

- **Temperature Cycle Test**

	Temperature
Operation	0°C
	70°C[Note1]
Storage	-40°C
	85°C

Notes:

1. Operation temperature is measured by device temperature sensor. Airflow is suggested and it will allow device to be operated at appropriate temperature for each component during heavy workloads environment.
2. Operation temperature shows in case temperature not ambient temperature.

3.1.2. Shock

- **Shock Specification**

	Acceleration Force
Non-Operational	1500G
Operational	1500G

3.1.3. Vibration

- **Vibration Specification**

	Condition	
	Frequency/Displacement	**Frequency/Acceleration**
Non-Operational	20Hz~80Hz/1.52mm	80Hz~2000Hz/20G

3.1.4. Drop

- **Drop Specification**

	Height of Drop	Number of Drop
Non-operational	80cm free fall	6 face of each unit

3.1.5. Bending

- **Bending Specification**

	Force	Action
Non-operational	≥ 20N	Hold 1min/5times

3.1.6. Electrostatic Discharge (ESD)

Specification	+/- 4KV
EN 55024, CISPR 24 EN 61000-4-2 and IEC 61000-4-2	Device functions are affected, but EUT will be back to its normal or operational state automatically.

3.1.7. EMI Compliance

Specification
EN 55032, CISPR 32 (CE) AS/NZS CISPR 32 (CE) ANSI C63.4 (FCC) VCCI-CISPR 32 (VCCI) CNS 13438 (BSMI)

3.2. MTBF

MTBF, Mean Time Between Failures, is a measure of reliability a device. Its value represents the average time between a repair and the next failure. The unit of MTBF is in hours. The higher the MTBF value, the higher the reliability of the device.

Our MTBF result is based on simulation software (Relex7.3). Please note that a lower MTBF should be expected for higher capacity drives, and we apply the lowest MTBF all capacities.

4. ELECTRICAL SPECIFICATIONS

4.1. Supply Voltage

Parameter	Rating
Operating Voltage	Min = 3.14V Max = 3.47V
Rise Time (Max/Min)	100ms / 0.1ms
Fall Time (Max/Min)	5s / 1ms
Min. off Time[Note1]	1s

Note:

1. Minimum time between power removed from SSD (Vcc < 100mW) and power re-applied to the drive.

4.2. Power Consumption

- Power consumption with Toshiba BiCS3 TLC in W

Capacity	Flash Structure	Flash Type	CE#	Read			Write		
				Peak	Max.	Avg.	Peak	Max.	Avg.
240/256GB	64GB x 4	TSB Bics3, BGA132	8	6.4	5.2	5.0	5.0	3.6	3.5
	128GB x 2	TSB Bics3, BGA272	8	7.6	6.4	6.1	5.6	3.9	3.5
480/512GB	128GB x 4	TSB Bics3, BGA132	16	6.6	5.5	5.3	5.8	4.1	3.9
	256GB x 2	TSB Bics3, BGA272	16	8.4	7.0	6.7	6.8	5.2	4.8
960GB/1TB	256GB x 4	TSB Bics3, BGA132	32	8.9	7.2	6.9	7.1	6.1	5.6
1920GB/2TB	512GB x 4	TSB Bics3, BGA152	32	7.2	5.9	5.7	8.0	6.1	6.0

Unit: W

Notes

1. Based on ECFM1xxx-series under ambient temperature.
2. Use CrystalDiskMark 5.1.2 with the setting of 1000MB. Sequentially read and write the disk for 5 times, and measure power consumption during sequential Read [1/5]~[5/5] or sequential Write [1/5]~[5/5]
3. Power Consumption may differ according to flash configuration and platform.
4. The measured power voltage is 3.3V.

- Power consumption with Toshiba BiCS3 TLC in mW

Capacity	Flash Structure	CE#	Active			PS3	PS4
			PS0	PS1	PS2		
120/128GB	64GB x 2	4	3,100	2,500	2,100	16	2
240/256GB	128GB x 2	8	5,300	4,000	2,900	16	2
480/512GB	256GB x 2	16	5,500	4,900	3,900	16	2
960GB/1TB	256GB x 4	32	5,300	5,200	4,700	16	2
1920GB/2TB	512GB x 4	32	5,700	5,100	4,700	16	2

Unit: mW

Notes

1. Based on ECFM1xxx-series under ambient temperature.
2. The average value of power consumption is achieved based on 100% conversion efficiency.
3. The measured power voltage is 3.3V.
4. The temperature of a storage device in PS1 should remain constant or should slightly decrease for all workloads so the actual power in PS1 should be lower than PS0.
5. The temperature of a storage device in PS2 should decrease sharply for all workloads so the actual power in PS2 should be lower than PS1.

- Mobile Mark 2014 Average Power consumption with Toshiba BiCS3 TLC

Capacity	Flash Structure	CE#	Primary
120/128GB	128GB x 1	4	TBA
240/256GB	128GB x 2	8	TBA
480/512GB	256GB x 2	16	TBA
960GB/1TB	512GB x 2	16	TBA
1920GB/2TB	1024GB x 2	32	TBA

Unit: mW

Notes

1. Based on ECFM1xxx-series under ambient temperature.
2. The measured power voltage is 3.3V.
3. The average value of power consumption is achieved based on 100% conversion efficiency.

5.1. Pin Assignment and Descriptions

The follow table defines the signal assignment of the internal NGFF connector for SSD usage, described in the PCI Express M.2 Specification version 1.1 of the PCI-SIG.

Pin #	SATA Pin	Description
1	GND	Ground
2	3.3V	3.3V source
3	GND	Ground
4	3.3V	3.3V source
5	PETn3	PCIe TX Differential signal defined by the PCI Express M.2 spec
6	N/C	No connect
7	PETp3	PCIe TX Differential signal defined by the PCI Express M.2 spec
8	N/C	No connect
9	GND	Ground
10	LED1#	Open drain, active low signal. These signals are used to allow the add-in card to provide status indicators via LED devices that will be provided by the system.
11	PERn3	PCIe RX Differential signal defined by the PCI Express M.2 spec
12	3.3V	3.3V source
13	PERp3	PCIe RX Differential signal defined by the PCI Express M.2 spec
14	3.3V	3.3V source
15	GND	Ground
16	3.3V	3.3V source
17	PETn2	PCIe RX Differential signal defined by the PCI Express M.2 spec
18	3.3V	3.3V source
19	PETp2	PCIe RX Differential signal defined by the PCI Express M.2 spec
20	N/C	No connect
21	GND	Ground
22	N/C	No connect
23	PERn2	PCIe RX Differential signal defined by the PCI Express M.2 spec
24	N/C	No connect
25	PERp2	PCIe RX Differential signal defined by the PCI Express M.2 spec
26	N/C	No connect
27	GND	Ground
28	N/C	No connect

Pin #	SATA Pin	Description
29	PETn1	PCIe TX Differential signal defined by the PCI Express M.2 spec
30	N/C	No connect
31	PETp1	PCIe TX Differential signal defined by the PCI Express M.2 spec
32	N/C	No connect
33	GND	Ground
34	N/C	No connect
35	PERn1	PCIe RX Differential signal defined by the PCI Express M.2 spec
36	N/C	No connect
37	PERp1	PCIe RX Differential signal defined by the PCI Express M.2 spec
38	N/C	No connect
39	GND	Ground
40	SMB_CLK (I/O)(0/1.8V)	SMBus Clock; Open Drain with pull-up on platform.
41	PETn0	PCIe TX Differential signal defined by the PCI Express M.2 spec
42	SMB_DATA (I/O)(0/1.8V)	SMBus Data; Open Drain with pull-up on platform.
43	PETp0	PCIe TX Differential signal defined by the PCI Express M.2 spec
44	ALERT#(O)(0/1.8V)	Alert notification to master; Open Drain with pull-up on platform; Active low.
45	GND	Ground
46	N/C	No connect
47	PERn0	PCIe RX Differential signal defined by the PCI Express M.2 spec
48	N/C	No connect
49	PERp0	PCIe RX Differential signal defined by the PCI Express M.2 spec
50	PERST#(I)(0/3.3V)	PE-Reset is a functional reset to the card as defined by the PCIe Mini CEM specification.
51	GND	Ground
52	CLKREQ#(I/O)(0/3.3V)	Clock Request is a reference clock request signal as defined by the PCIe Mini CEM specification; Also used by L1 PM Sub-states.
53	REFCLKn	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
54	PEWAKE#(I/O)(0/3.3V)	PCIe PME Wake. Open Drain with pull up on platform; Active Low.
55	REFCLKp	PCIe Reference Clock signals (100 MHz) defined by the PCI Express M.2 spec.
56	Reserved for MFG DATA	Manufacturing Data line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.

Pin #	SATA Pin	Description
57	GND	Ground
58	Reserved for MFG CLOCK	Manufacturing Clock line. Used for SSD manufacturing only. Not used in normal operation. Pins should be left N/C in platform Socket.
59	Module Key M	Module Key
60	Module Key M	
61	Module Key M	
62	Module Key M	
63	Module Key M	
64	Module Key M	
65	Module Key M	
66	Module Key M	
67	N/C	No Connect
68	SUSCLK(32KHz) (I)(0/3.3V)	32.768 kHz clock supply input that is provided by the platform chipset to reduce power and cost for the module.
69	N/C	PEDET (NC-PCIe). No Connect for PCIe.
70	3.3V	3.3V source
71	GND	Ground
72	3.3V	3.3V source
73	GND	Ground
74	3.3V	3.3V source
75	GND	Ground

6. SUPPORTED COMMANDS

6.1. NVMe Command List

Table 6-1 Admin Commands

Op-Code	O/M	Command Description
00h	M	Delete I/O Submission Queue
01h	M	Create I/O Submission Queue
02h	M	Get Log Page
04h	M	Delete I/O Completion Queue
05h	M	Create I/O Completion Queue
06h	M	Identify
08h	M	Abort
09h	M	Set Features
0Ah	M	Get Features
0Ch	M	Asynchronous Event Request
10h	O	Firmware Activate
11h	O	Firmware Image Download
14h	O	Device Self-test
80h	O	Format NVM
81h	O	Security Send
82h	O	Security Receive
84h	O	Sanitize

Table 6-2 I/O Commands

Op-Code	O/M	Command Description
00h	O	Flush
01h	O	Write
02h	O	Read
04h	O	Write Uncorrectable
05h	O	Compare
08h	O	Write Zeroes
09h	O	Dataset Management

Table 6-3 Set Feature Commands

Op-Code	O/M	Command Description
00h		Reserved
01h	M	Arbitration
02h	M	Power Management
03h	O	LBA Range Type
04h	M	Temperature Threshold
05h	M	Error Recovery
06h	O	Volatile Write Cache
07h	M	Number of Queues
08h	M	Interrupt Coalescing
09h	M	Interrupt Vector Configuration
0Ah	M	Write Atomicity Normal
0Bh	M	Asynchronous Event Configuration
0Ch	O	Autonomous Power State Transition
0Dh	O	Host Memory Buffer
0Eh	O	Timestamp
10h	O	Host Controlled Thermal Management
11h	O	Non-Operational Power State Config
0Eh – 7Dh		Reserved
80h	O	Software Progress Marker

Table 6-4 Get Log Page Commands

Op-Code	O/M	Command Description
00h		Reserved
01h	M	Error Information
02h	M	SMART / Health Information
03h	M	Firmware Slot Information
04h	O	Changed Namespace List
06h	O	Device Self-test
09h – 7Fh		Reserved
81h	O	Sanitize Status
82h - FFh		Reserved

6.2. Identify Device Data

The following table details the sector data returned by the IDENTIFY DEVICE command.

■ **Identify Controller Data Structure**

Bytes	O/M	Default Value	Description
01:00	M	0x1987	PCI Vendor ID (VID)
03:02	M	0x1987	PCI Subsystem Vendor ID (SSVID)
23:04	M	TBD	Serial Number (SN)
63:24	M	TBD	Model Number (MN)
71:64	M	TBD	Firmware Revision (FR)
72	M	0x01	Recommended Arbitration Burst (RAB)
75:73	M	TBD *	IEEE OUI Identifier (IEEE)
76	O	0x00	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)
77	M	0x09	Maximum Data Transfer Size (MDTS)
79:78	M	0x0001	Controller ID (CNTLID)
83:80	M	0x00010300	Version (VER)
87:84	M	0x001E8480(2sec)	RTD3 Resume Latency (RTD3R)
91:88	M	0x00989680(10sec)	RTD3 Entry Latency (RTD3E)
95:92	M	0x00000300	Optional Asynchronous Events Supported (OAES)
99:96	M	0x0002	Controller Attributes (CTRATT)
239:100	-	0x00	Reserved
255:240	-	0x00	Refer to the NVMe Management Interface Specification for definition
257:256	M	0x0017	Optional Admin Command Support (OACS)
258	M	0x03	Abort Command Limit (ACL)
259	M	0x03	Asynchronous Event Request Limit (AERL)
260	M	0x1F	Firmware Updates (FRMW)
261	M	0x0C	Log Page Attributes (LPA)
262	M	0x3E	Error Log Page Entries (ELPE)
263	M	4	Number of Power States Support (NPSS)
264	M	0x01	Admin Vendor Specific Command Configuration (AVSCC)
265	O	0x01	Autonomous Power State Transition Attributes (APSTA)
267:266	M	0x0157 (70C)	Warning Composite Temperature Threshold (WCTEMP)
269:268	M	0x0161 (80C)	Critical Composite Temperature Threshold (CCTEMP)
271:270	O	0x0000 (No report)	Maximum Time for Firmware Activation (MTFA)
275:272	O	0x00000000	Host Memory Buffer Preferred Size (HMPRE)
279:276	O	0x00000000	Host Memory Buffer Minimum Size (HMMIN)

Bytes	O/M	Default Value	Description
295:280	O	**	Total NVM Capacity (TNVMCAP)
311:296	O	**	Unallocated NVM Capacity (UNVMCAP)
315:312	O	0x00000000	Replay Protected Memory Block Support (RPMBS)
511:316	-	Non-zero	Reserved
NVM Command Set Attributes			
512	M	0x66	Submission Queue Entry Size (SQES)
513	M	0x44	Completion Queue Entry Size (CQES)
515:514	-	0x0000	Reserved
519:516	M	0x00000001	Number of Namespaces (NN)
521:520	M	0x001F	Optional NVM Command Support (ONCS)
523:522	M	0x0000	Fused Operation Support (FUSES)
524	M	0x00	Format NVM Attributes (FNA)
525	M	0x01	Volatile Write Cache (VWC)
527:526	M	TBD	Atomic Write Unit Normal (AWUN)
529:528	M	TBD	Atomic Write Unit Power Fail (AWUPF)
530	M	0x01	NVM Vendor Specific Command Configuration (NVSCC)
531	-	0x00	Reserved
533:532	O	0x0000	Atomic Compare & Write Unit (ACWU)
535:534	-	0x0000	Reserved
539:536	O	0x00000000	SGL Support (SGLS)
703:540	-	0x00	Reserved
IO Command Set Attributes			
2047:704	-	0x00	Reserved
2079:2048	M	TBD	Power State 0 Descriptor (PSD0)
2111:2080	O	0x00	Power State 1 Descriptor (PSD1)
2143:2112	O	0x00	Power State 2 Descriptor (PSD2)
2175:2144	O	0x00	Power State 3 Descriptor (PSD3)
2207:2176	O	0x00	Power State 4 Descriptor (PSD4)
2239:2208	O	0x00	Power State 5 Descriptor (PSD5)
2271:2240	O	0x00	Power State 6 Descriptor (PSD6)
2303:2272	O	0x00	Power State 7 Descriptor (PSD7)
2335:2304	O	0x00	Power State 8 Descriptor (PSD8)
2367:2336	O	0x00	Power State 9 Descriptor (PSD9)
2399:2368	O	0x00	Power State 10 Descriptor (PSD10)
2431:2400	O	0x00	Power State 11 Descriptor (PSD11)

Bytes	O/M	Default Value	Description
2463:2432	O	0x00	Power State 12 Descriptor (PSD12)
2495:2464	O	0x00	Power State 13 Descriptor (PSD13)
2527:2496	O	0x00	Power State 14 Descriptor (PSD14)
2559:2528	O	0x00	Power State 15 Descriptor (PSD15)
2591:2560	O	0x00	Power State 16 Descriptor (PSD16)
2623:2592	O	0x00	Power State 17 Descriptor (PSD17)
2655:2624	O	0x00	Power State 18 Descriptor (PSD18)
2687:2656	O	0x00	Power State 19 Descriptor (PSD19)
2719:2688	O	0x00	Power State 20 Descriptor (PSD20)
2751:2720	O	0x00	Power State 21 Descriptor (PSD21)
2783:2752	O	0x00	Power State 22 Descriptor (PSD22)
2815:2784	O	0x00	Power State 23 Descriptor (PSD23)
2847:2816	O	0x00	Power State 24 Descriptor (PSD24)
2879:2848	O	0x00	Power State 25 Descriptor (PSD25)
2911:2880	O	0x00	Power State26 Descriptor (PSD26)
2943:2912	O	0x00	Power State 27 Descriptor (PSD27)
2975:2944	O	0x00	Power State 28 Descriptor (PSD28)
3007:2976	O	0x00	Power State 29 Descriptor (PSD29)
3039:3008	O	0x00	Power State 30 Descriptor (PSD30)
3071:3040	O	0x00	Power State 31 Descriptor (PSD31)
Vendor Specific			
4095:3072	O	Vendor Reserved	Vendor Specific (VS)

***** The OUI shall be a valid IEEE/RAC assigned identifier that may be registered at http://standards.ieee.org/develop/regauth/oui/public.html.

****** Depends on the using of capacity

Identify Namespace Data Structure & NVM Command Set Specific

Bytes	O/M	Default Value	Description
7:0	M	TBD*	Namespace Size (NSZE)
15:8	M	TBD*	Namespace Capacity (NCAP)
23:16	M	TBD*	Namespace Utilization (NUSE)
24	M	0x00	Namespace Features (NSFEAT)
25	M	0x01	Number of LBA Formats (NLBAF)
26	M	0x00	Formatted LBA Size (FLBAS)
27	M	0x00	Metadata Capabilities (MC)
28	M	0x00	End-to-end Data Protection Capabilities (DPC)
29	M	0x00	End-to-end Data Protection Type Settings (DPS)
30	O	0x00	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)
31	O	0x00	Reservation Capabilities (RESCAP)
32	O	0x00	Format Progress Indicator (FPI)
33	-	0x00	Reserved
35:34	O	0x0000	Namespace Atomic Write Unit Normal (NAWUN)
37:36	O	0x0000	Namespace Atomic Write Unit Power Fail (NAWUPF)
39:38	O	0x0000	Namespace Atomic Compare & Write Unit (NACWU)
41:40	O	0x0000	Namespace Atomic Boundary Size Normal (NABSN)
43:42	O	0x0000	Namespace Atomic Boundary Offset (NABO)
45:44	O	0x0000	Namespace Atomic Boundary Size Power Fail (NABSPF)
47:46	-	0x0000	Reserved
63:48	O	0x00	NVM Capacity (NVMCAP)
103:64	-	0x00	Reserved
119:104	O	TBD **	Namespace Globally Unique Identifier (NGUID)
127:120	O	TBD **	IEEE Extended Unique Identifier (EUI64)
131:128	M	0x02090000	LBA Format 0 Support (LBAF0)
135:132	O	0x00000000	LBA Format 1 Support (LBAF1)
139:136	O	0x00000000	LBA Format 2 Support (LBAF2)
143:140	O	0x00000000	LBA Format 3 Support (LBAF3)
147:144	O	0x00000000	LBA Format 4 Support (LBAF4)
151:148	O	0x00000000	LBA Format 5 Support (LBAF5)
155:152	O	0x00000000	LBA Format 6 Support (LBAF6)
159:156	O	0x00000000	LBA Format 7 Support (LBAF7)
163:160	O	0x00000000	LBA Format 8 Support (LBAF8)
167:164	O	0x00000000	LBA Format 9 Support (LBAF9)

Bytes	O/M	Default Value	Description
171:168	O	0x00000000	LBA Format 10 Support (LBAF10)
175:172	O	0x00000000	LBA Format 11 Support (LBAF11)
179:176	O	0x00000000	LBA Format 12 Support (LBAF12)
183:180	O	0x00000000	LBA Format 13 Support (LBAF13)
187:184	O	0x00000000	LBA Format 14 Support (LBAF14)
191:188	O	0x00000000	LBA Format 15 Support (LBAF15)
383:192	-	0x00	Reserved
4095:384	O	0x00	Vendor Specific (VS)

* See IDEMA SPEC

** See IEEE EUI-64 SPEC

■ **List of Identify Namespace Data Structure for Each Capacity**

Capacity (GB)	Byte[7:0]: Namespace Size (NSZE)
120	DF94BB0h
128	EE7C2B0h
240	1BF244B0h
256	1DCF32B0h
480	37E436B0h
512	3B9E12B0h
960	6FC81AB0h
1024	773BD2B0h
1920	DF8FE2B0h
2048	EE7752B0h

6.3. SMART Attributes

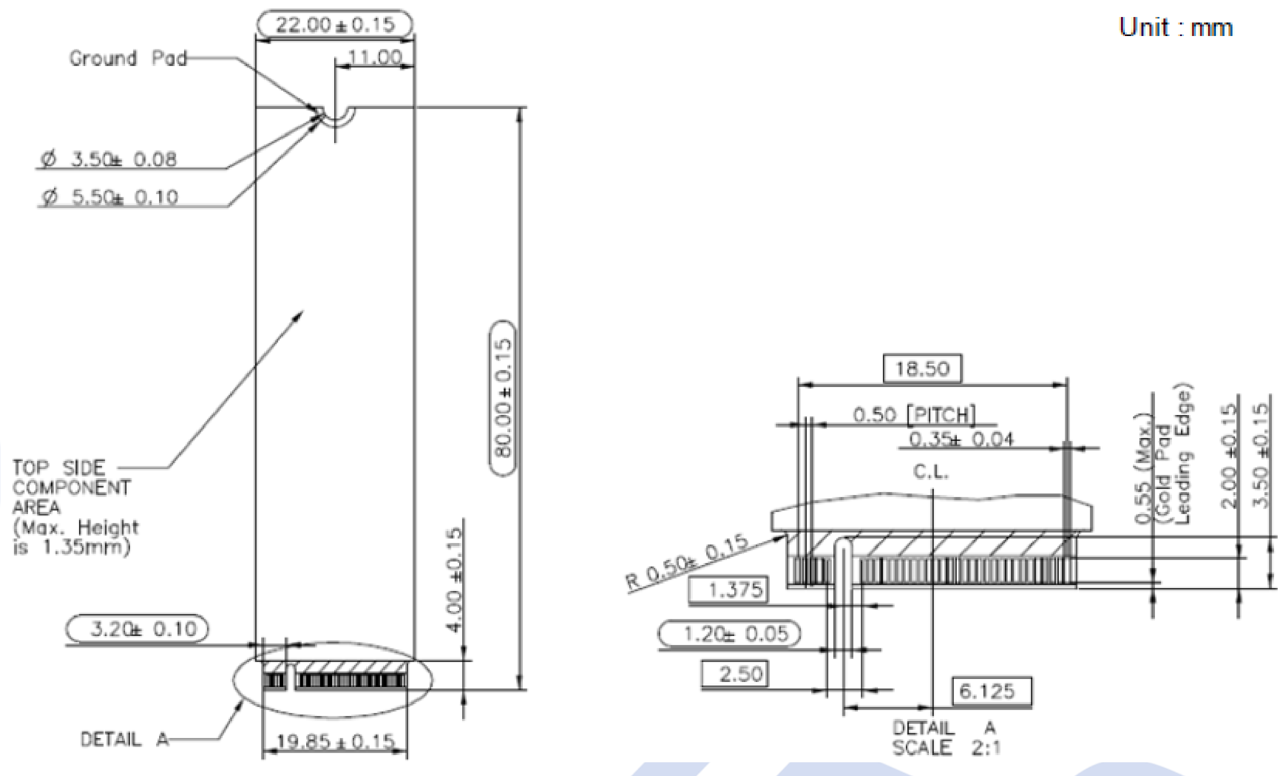
■ **SMART Attributes (Log Identifier 02h)**

Bytes Index	Bytes	Description
[0]	1	Critical Warning
[2:1]	2	Composite Temperature
[3]	1	Available Spare
[4]	1	Available Spare Threshold
[5]	1	Percentage Used
[31:6]	26	Reserved
[47:32]	16	Data Units Read
[63:48]	16	Data Units Written
[79:64]	16	Host Read Commands
[95:80]	16	Host Write Commands
[111:96]	16	Controller Busy Time
[127:112]	16	Power Cycles
[143:128]	16	Power On Hours
[159:144]	16	Unsafe Shutdowns
[175:160]	16	Media and Data Integrity Errors
[191:176]	16	Number of Error Information Log Entries
[195:192]	4	Warning Composite Temperature Time
[199:196]	4	Critical Composite Temperature Time
[201:200]	2	Temperature Sensor 1 (Current Temperature)
[203:202]	2	Temperature Sensor 2 (N/A)
[205:204]	2	Temperature Sensor 3 (N/A)
[207:206]	2	Temperature Sensor 4 (N/A)
[209:208]	2	Temperature Sensor 5 (N/A)
[211:210]	2	Temperature Sensor 6 (N/A)
[213:212]	2	Temperature Sensor 7 (N/A)
[215:214]	2	Temperature Sensor 8 (N/A)
[511:216]	296	Reserved

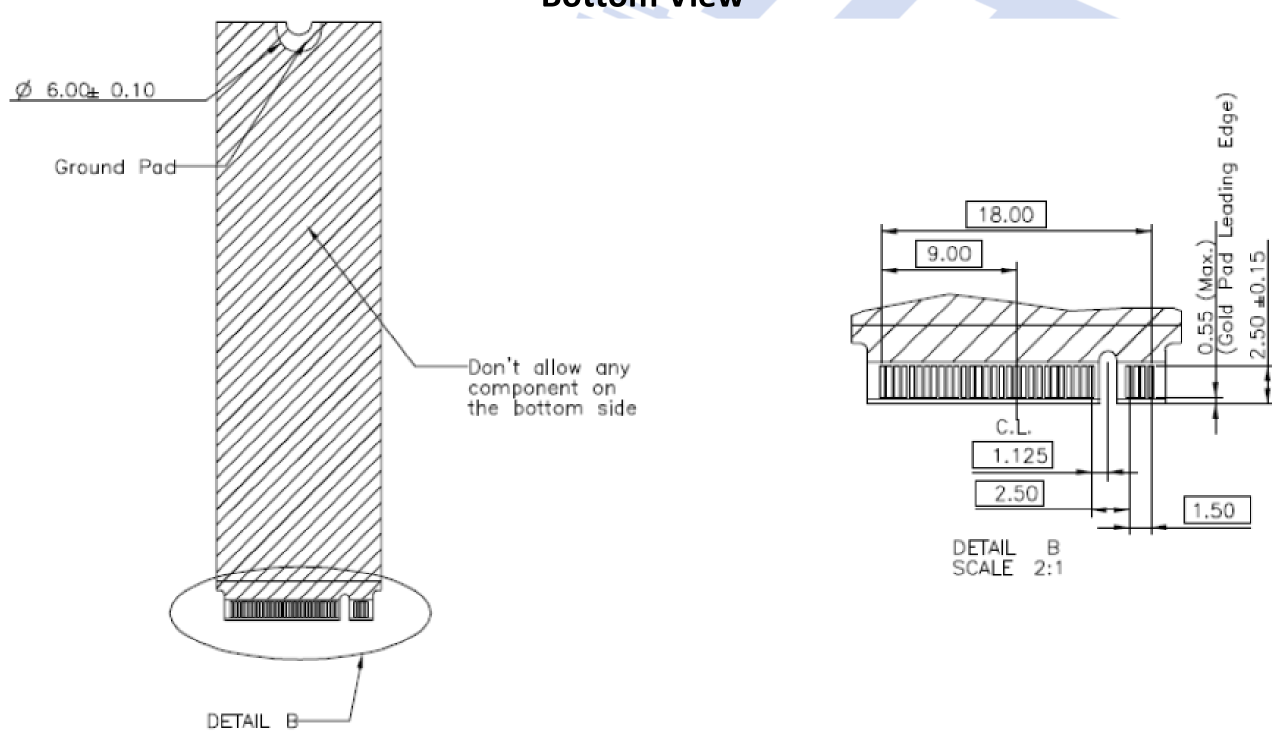
7. PHYSICAL DIMENSION

- **Dimension of M.2 2280-S2-M: 80mm(L) x 22mm(W) x 1.35mm(H)**
  Physical Product Dimension: 80mm(L) x 22mm(W) x 1.20mm(H)

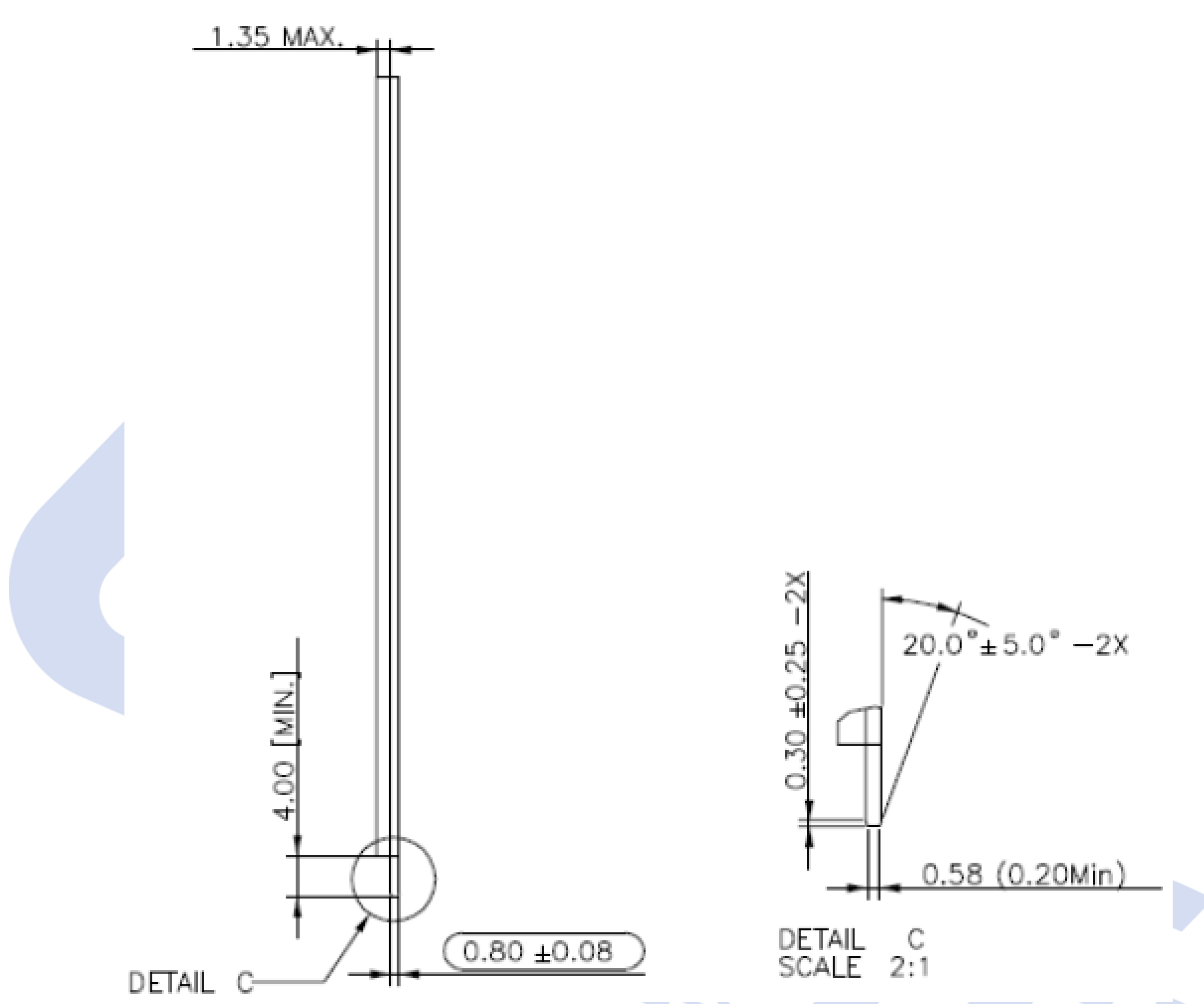
Top View



Bottom View



Side View



***Notes:**

1. =Max Component Height
2. =No Component
3. =No Component / Signal Vias / Signal Copper / Printing
4. General Tolerance: ±0.15mm
5. is IQC inspection dimension

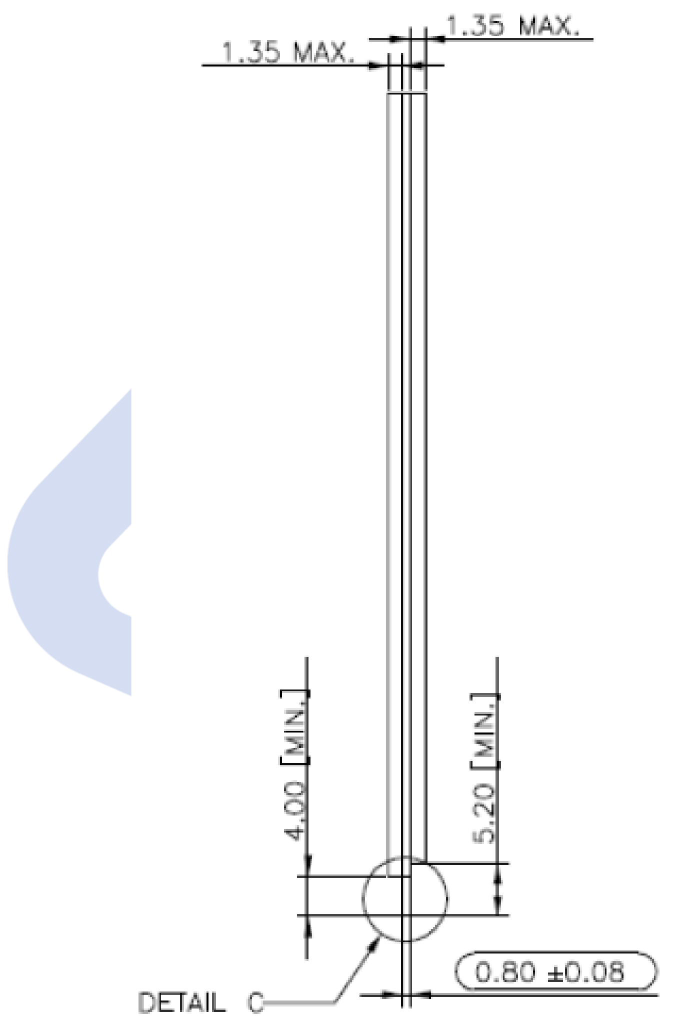
- **Dimension of M.2 2280-D2-M: 80mm(L) x 22mm(W) x 3.5mm(H)**

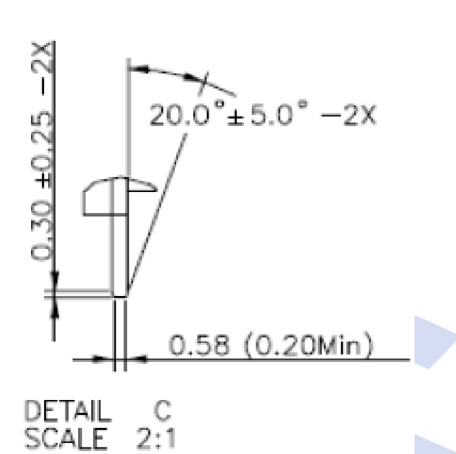
Top View

Unit : mm

Bottom View

Side View





***Notes:**

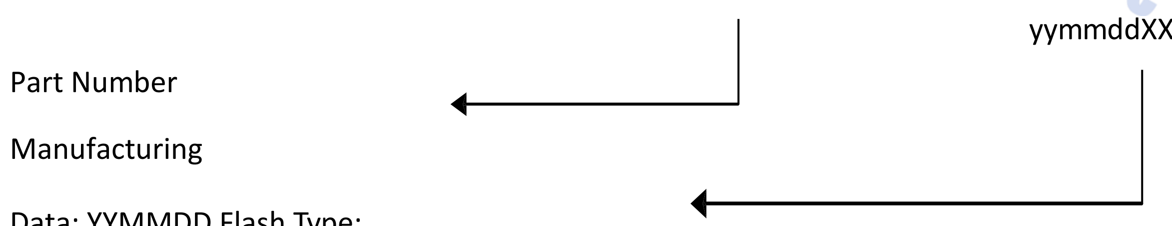
1. =Max Component Height
2. =No Component
3. =No Component / Signal Vias / Signal Copper / Printing
4. General Tolerance: ±0.15mm
5. is IQC inspection dimension

8. TERMINOLOGY

The following table is to list out the acronyms that have been applied throughout the document.

Term	Definitions
ATTO	Commercial performance benchmark application
DDR	Double data rate (SDRAM)
ASPM	Active States Power Management
APST	Autonomous Power State Transition
LBA	Logical block addressing
MTBF	Mean time between failures
PCIe	PCI Express / Peripheral Component Interconnect Express
S.M.A.R.T.	Self-monitoring, analysis and reporting technology

9. BARCODE DESCRIPTION



10. PARTNUMBER DECODER

M2P-80UB$X^8X^9X^{10}X^{11}X^{12}X^{13}X^{14}X^{15}X^{16}X^{17}$

$X^1X^2X^3$	X^4X^5	X^6X^7	$X^8 X^9 X^{10} X^{11} X^{12}$		X^{13}	X^{14}	X^{15}	$X^{16}X^{17}$
M2P	80	UB	120GB 240GB 480GB 960GB 1920G	128GB 256GB 512GB 001TB 002TB	A: 3D TLC Standard (0ºC ~ +70ºC)	E	P	blank