

### **TFT-Display Datasheet**

# FG1001T0DSSWNG01| Datalmage

### **Features**

Active Screen Area	216.81x135.5 [mm]
Size   Format	10,1"   16:10
Resolution	1920x1200
Backlight	LED
Brightness	800 cd/m <sup>2</sup>
LED Life Time	20K (h)
Interface	MIPI
Viewing Angle	L/R 85/85 - U/D 85/85
Touchscreen	no
Power Supply	3.3V [Typ.]
Module Outline	229.4x150.0x2.9 [mm]
Operation Temperature	-10 + 60°C
Storage Temperature	-20 + 70°C

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# DATA IMAGE CORPORATION

	TFT Module Specification ITEM NO.: <u>FG1001T0DSSWNG01</u> ■Prototype □Pre-prod. □Mass prod. Table of Contents	
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Customer Companies	QA Approval	QA Check	R&D Approval	R&D Check
	pretty	Andy	Dragon	Andrew
Approved by	Version:	Issued Date:	Total Pages::	Prepared by
	1	08/MAR/19'	28	Candy



### 2. RECORD OF REVISION

Rev	Date	Item	Page	Comment	Source
1	08/MAR/19'			Initial PRELIMINARY	ESR0802035



### **3. GENERAL SPECIFICATIONS**

Parameter	Specifications	Unit			
Screen Size	10.1 (diagonal)	inch			
Display resolution	1920(H) x (R,G,B) x 1200(V)	dot			
Active Area	216.81(H) × 135.5(V)	mm			
Pixel Pitch	0.1129(H) × 0.1129(V)	mm			
Pixel Arrangement	R.G.B. Vertical Stripe				
Outline Dimension	229.4(H) ×150(V) ×2.9(D)	mm			
Surface treatment	Glare				
Electrical Interface	MIPI				
Weight	TBD	g			
Display mode	AHVA, Normally Black				
our components and processes are compliant to RoHS standard					

### 4. ABSOLUTE MAXIMUM RATINGS

An absolute maximum rating of the module is as following:

### 4.1Absolute Ratings of TFT LCD Module

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Logic/LCD drive Voltage	Vin	-0.3	+4.5	[Volt]	Note 1,2

### **4.2Absolute Ratings of Environment**

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Operating Temperature	TOP	-10	+60	[°C]	
Operation Humidity	HOP	5	90	[%RH]	
Storage Temperature	TST	-20	+70	[°C]	
Storage Humidity	HST	5	90	[%RH]	

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: Maximum wet-bulb temperature is less than 39 °C and no condensation

Note 4: Operating temperature means "Front and rear surface" of panel

### 5. ELECTRICAL CHARACTERISTIC

### 5.1 TFT LCD Module

### 5.1.1 Power Specification

Input power specifications are as follows;

The power specification are measured under 25 and frame frequency under 60Hz

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Logic/LCD Drive Voltage	VDD	3.0	3.3	4.2	[Volt]	
VDD Power	PDD	-	-	0.95	[Watt]	Note 1
IDD Current	IDD	-	-	316	[mA]	Note 1
Inrush Current	IRush	-	-	2000	[mA]	Note 2
Allowable Logic/LCD Drive Ripple Voltage	VDDrp	-	-	100	[mV] p-p	Note 2

Note 1 : Maximum Measurement Condition: White Pattern at 3.3V driving voltage. (Pmax=V3.3 x Iwhite)

Note 2: Measure Condition



### **VDD** rising time

**5.1.2 Signal Electrical Characteristics** Input signals shall be low or High-impedance state when VDD is off. MIPI DC/AC Characteristics are as follows;

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Input data bit rate	BRMIPI	200	-	1000	Mbps
Common-mode voltage(HS Rx mode)	VCMRX	70	-	330	mV
Differential input high threshold (HS Rx mode)	Vidth	-	-	70	mV
Differential input low threshold (HS Rx mode)	Vidtl	-70	-	-	mV
Differential input voltage range (HS Rx mode)	Vidm	70	-	500	mV
Single-end input high voltage (HS Rx mode)	VIHHS	-	-	460	mV
Single-end input low voltage (HS Rx mode)	VILHS	-40	-	-	mV
Differential input impedance	Zid	80	100	125	Ω
Logic 1 input voltage (LP Rx mode)	Vihlp	880			mV
Logic 0 input voltage (LP Rx mode)	VILLP			550	mV
Output high level (LP Tx mode)	Vон	1.08	1.2	1.32	V
Output low level (LP Tx mode)	Vol	-50		50	mV







HS Differential Signaling

LP Single-ended Signaling

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Common-mode interference beyond 450MHz	$\triangle V_{CMRX(HF)}$		-	-	100	mV
Common-mode interference 50MHz ~ 450MHz	$\triangle V_{CMRX(LF)}$		-50	-	50	mV
Common-mode termination	Ссм		-	-	60	pF
UI instantaneous	UIINST		1	-	12.5	ns

HS RX Scheme





Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Notes
Data to Clock Skew (mesured at transmitter)	Tskew[tx]	-0.15	-	0.15	UIINST	Note1
Data to Clock Setup Time (receiver)	TSETUP[RX]	0.15		-	UIINST	Note2
Data to Clock Hold Time (receiver)	THOLD[RX]	0.15	-	-	UIINST	Note2

Note:

1. Total silicon and package delay budget of 0.3\*UIINST

2. Total setup and hold window for receiver of 0.3\*UINST

High Speed Data Transmission: Data to Clock Timing



Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input pulse rejection	<b>E</b> SPIKE		-	-	300	V.ps
Minimum pulse width response	Tmin-rx		50	-	-	ns
Peak interference amplitude	Vint		-	-	200	mV
Interference frequency	fint		450	-	-	MHz

Input Glitch Rejection of Low-Power Receivers



For MIPI data transmission from TX to TCON works properly in video mode, it is suggested that all of MIPI

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lanes

status follow the scheme showed in below. When power is turned on, all lanes (include clock lane) are into LP-11

status first. When TX wants to start transmitting data to TCON, the clock lane is into HS and start toggling. Then data

lanes are into HS and data are transmitted. After data transmissions are finished (ex. H-blanking, V-blanking), the

data lanes are returned to LP-11, then clock lane, too. The transmission start from LP-11 and stop in LP-11 on all

lanes (include clock lane) are the recommended proper operation sequence for MIPI video mode.



#### The timing definitions are listed in below,

Parameter Description		MIN.	TYP.	MAX.	Unit
TCLK-MISS	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.				ns
Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.		8			UI
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
TCLK-SETTLE	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.	95		300	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.			38	ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time			35 ns + 4*UI	ns

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	point when				
	Dn crosses VIL,MAX.				
TEOT	TEOT TEOT TEOT TEOT TEOT TEOT TEOT TEOT			105 ns + 12*UI	ns
THS-EXIT	XIT Time that the transmitter drives LP-11 following a HS burst.				ns
THS-SYNC	HS Sync-Sequence '00011101' period		8		UI
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + 4*UI		85 ns + 6*UI	ns
THS-PREPARE + THS-ZERO	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI			ns
THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE.	85 ns + 6*UI		145ns + 10*UI	ns
THS-SKIP	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55 ns + 4*UI	ns
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60 ns + 4*UI			ns
TLPX	Transmitted length of any Low-Power state period	50			ns
Ratio TLPX	Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	2/3		3/2	
TTA-GET	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	5*TLPX			ns
TTA-GO	Time that the transmitter drives the Bridge state(LP-00) before releasing control during a Link Turnaround.		4*TLPX		ns
TTA-SURE	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX		2*TLPX	ns

Note:

2. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

High-Speed Data Transmission in Bursts

<sup>1.</sup> The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.



Switching the Clock Lane between Clock Transmission and Low-Power Mode



**Turnaround Procedure** 



### 5.2 Backlight Unit 5.2.1 LED characteristics

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Backlight Power Consumption	PLED	-	-	4.9	[Watt]	(Ta=25℃ @800nits)
LED Life-Time	N/A	15,000	20,000	-	Hour	(Ta=25℃ @800nits) Note1
LED Forward Voltage	VF	5.5	5.65	5.8	[Volt]	(Ta=25℃)
LED Forward Voltage of every LED string	VF-string	-	-	34.8	[Volt]	(Ta=25℃) Note2
LED Forward Current	IF	-	20	-	[mA]	(Ta=25℃)

Note 1. The LED life-time define as the estimated time to 50% degradation of initial luminous.

Note2. LED Array 6 parallel \* 6 series

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
LED Power Supply	VLED	3		12	[Volt]	
LED Enable Input High Level		1.7	-	5.5	[Volt]	
LED Enable Input Low Level	VLED_EN	-	-	0.8	[Volt]	Define as Connector
PWM Logic Input High Level	VPWM_E	1.7	-	5.5	[Volt]	Interface (Ta=25℃)
PWM Logic Input Low Level	N	-	-	0.8	[Volt]	Note1
PWM Input Frequency	FPWM	200	-	10K	Hz	
PWM Duty Ratio	Duty	1		100	%	

### 5.2.2 Backlight input signal characteristics

Note 1: The input high level voltage conversion to 2.5V by level shift circuit. Note 2: The LED PWM Logic Input Low Level Voltage must have an output impedance close to 0 ohm in front of input connector.



### 6. INPUT SIGNAL CHARACTERISTICS

### 6.1 Timing Characteristics

Basically, interface timings should match the 1920x1200 /60Hz manufacturing guide line timing.

P	arameter	Symbol	MIN.	TYP.	MAX.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequ	ency	1/ TClock	148.04	149.9	151.27	MHz
Vertical Section	Period	T∨	1206	1212	1218	
	Active	Tvd		TLine		
	Blanking	Тув	6	12	18	
Llorizontol	Period	Тн	2046	2058	2070	
Section	Active	Тно	1920			TClock
	Blanking	Тнв	126	138	150	

Note : DE mode only

### 6.1.2 Timing diagram



### 6.2 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.





Power Sequence Timing					
Denemeter	Va	lue	Units		
Parameter	MIN.	MAX.	01113		
T1	0.5	10			
T2	40	-			
T5	120	-			
Т6	50	-			
T7	0	-			
Т8	0	10			
T11	500	-	1115		
T12	10	-			
T13	10	-			
T14	0.5	10			
T15	10	-			
T18	10	-			

Note: LED\_PWM must be pull low(GND) when it is not pull high.

### 6.3 Signal Interface Characteristic 6.3.1 Pixel Format Image

Following figure shows the relationship between input signal and LCD pixel format.





### 6.3.2 The Input Data Format

Input Pixel Stream Format (1920RGB in 4 Lanes with RGB 8-8-8 format)



LPS : Low Power State

SoT : Start of Transmission

EoT : End of Transmission

ECC : Error-Correcting Code

### 6.4 Integration Interface Requirement

### 6.4.1 MIPI Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

<b>Connector Name / Designation</b>	For Signal Connector
Manufacturer	HIROSE
Type / Part Number	FH34SJ-34S-0.5SH(50) or compatible
Mating Housing/Part Number	FPC Cable



### 7. OPTICAL CHARACTERISTIC

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks	
	[degree]	Horizontal (Right) CR = 10 (Left)	80	85	-			
Viewing Angle	[degree]	Horizontal (Right) CR = 10 (Left)	80	85	-	dog	Note 1.4	
(CR≥10)	[degree]	Vertical (Upper) CR = 10 (Lower)	(Upper) (Lower) 80 85 -	ueg	NOLE 1,4			
	[degree]	Vertical (Upper) CR = 10 (Lower))	80	85	-			
Contrast Ratio	CR	Normal	600	800	-		Note 1,3	
Response time	Ton	θ=Φ=0°	-	25	35	ms	Note 1,6	
	Red x		TBD	TBD	TBD	-	Note 1.7	
	Red y		TBD	TBD	TBD	-		
	Green x		TBD	TBD	TBD			
Color chromaticity	Green y		TBD	TBD	TBD			
Color enronnationly	Blue x		TBD	TBD	TBD			
	Blue y		TBD	TBD	TBD			
	White x		TBD	TBD	TBD			
	White y		TBD	TBD	TBD			
Luminance	L		600	800	-	Cd/m <sup>²</sup>	Note 1,2	
Luminance uniformity	B-uni	5 points	70		-	%	Note1,5	
Image sticking		tis			2	Sec	Note 8	

The following optical specifications shall be measured in a darkroom or equivalent state (ambient luminance  $\leq 1$  lux, and at room temperature). The operation temperature is  $25^{\circ}C\pm 2^{\circ}C$ . The measurement method is shown in Note1.

Note1: The method of optical measurement:



Note2: Measured at the center area of the panel and at the viewing angle of the  $\theta x=\theta y=0^{\circ}$ Note3: Definition of Contrast Ratio (CR):

CR = Luminance with all pixels in white state Luminance with all pixels in Black state

Note4: Definition of Viewing Angle





#### Note 5: Definition of Brightness Uniformity (B-uni):





Note6: Definition of Response Time:

The Response Time is set initially by defining the "Rising Time (Tr)" and the "Falling Time (Tf)" respectively. Tr and Tf are defined as following figure.



 Image
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 Data input
 White
 Black
 White

 Image
 Image
 Image
 Image
 Image

 Image
 Image
 Image
 Image
 Image

Note 7: Definition of Chromaticity:

The color coordinates  $(x_W, y_W), (x_R, y_R), (x_G, y_G)$ , and  $(x_B, y_B)$  are obtained with all pixels in the viewing field at white, red, green, and blue states, respectively.

Note 8: Definition of Image sticking (tis):

Continuously display the test pattern shown in the figure below for 2 hours. Then display a completely white screen. The previous image shall not persist more than 2 sec at 25 °C





Pin No	Symbol	Function	Remark
1	VDD	DC-DC circuit supply voltage	
2	VDD	DC-DC circuit supply voltage	
3	Hsync	Yoe signal output to system	
4	LED_EN	LED driver Enable Input	
5	LED_PWM	Backlight LED driver PWM Input	
6	ID	Pull high (10Kohm to 1.8V)	
7	ID	Pull high (10Kohm to 1.8V)	
8	NC	Not Connection	
9	GND	Ground	
10	DSI_D2P/Rx-IN2P	MIPI data pair 2 positive signal	
11	DSI_D2N/Rx-IN2N	MIPI data pair 2 negative signal	
12	GND	Ground	
13	DSI_D1P/Rx-IN1P	MIPI data pair 1 positive signal	
14	DSI_D1N/Rx-IN1N	MIPI data pair 1 negative signal	
15	GND	Ground	
16	DSI_CLKP/Rx-CLKP	MIPI Clock positive signal	
17	DSI_CLKN/Rx-CLKN	MIPI Clock negative signal	
18	GND	Ground	
19	DSI_D0P/Rx-IN0P	MIPI data pair 0 positive signal	
20	DSI_D0N/Rx-IN0N	MIPI data pair 0 negative signal	
21	GND	Ground	
22	DSI_D3P/Rx-IN3P	MIPI data pair 3 positive signal	
23	DSI_D3N/Rx-IN3N	MIPI data pair 3 negative signal	
24	GND	Ground	
25	GND	Ground	
26	GND	Ground	
27	GND	Ground	
28	ID	Pull low (4.7Kohm to Ground)	
29	Aging	Aging Mode Power Supply (AUO only)	
30	NC	Not Connection	



31	LED+	LED Power Supply	
32	LED+	LED Power Supply	
33	LED+	LED Power Supply	
34	LED+	LED Power Supply	







### 10.1 Test Condition

- 10.1.1 Temperature and Humidity(Ambient Temperature)
  - Temperature :  $25 \pm 5^{\circ}C$ Humidity :  $65 \pm 5\%$
- 10.1.2 Operation

Unless specified otherwise, test will be conducted under function state.

### 10.1.3 Container

Unless specified otherwise, vibration test will be conducted to the product itself without putting it in a container.

### 10.1.4 Test Frequency

In case of related to deterioration such as shock test. It will be conducted only once.

	Reliability Test Item & Level					
No.	Item	Test Conditions	Remark			
1	High Temperature Storage Test	Ta = 70°C 300Hr	IEC60068-2-2			
2	Low Temperature Storage Test	Ta = -20℃ 300Hr	IEC60068-2-1			
3	High Temperature Operation Test	Ts = 60°C 300Hr	IEC60068-2-2			
4	Low Temperature Operation Test	Ta = -10℃ 300Hr	IEC60068-2-1			
5	Operate at High Temperature and Humidity	40 °C /90%,300Hr	IEC60068-2-3			
6	Thermal Shock	-10 ℃ /30 min , 60 ℃ /30 min , 20cycles	IEC60068-2-14			
7	Vibration Test	Acceleration: 1.5 G Frequency: 10 - 500Hz Random Sweep: 30 Minutes each Axis (X, Y, Z) Test method: Non-Operation	IEC60068-2-6			
8	Drop test (Package)	Height :60cm 1 conner,3edges,6surfaces	IEC60068-2-32			
9	ESD	State: operating Location: LCM/TP surface Condition:150pf 330Ω Contact +/- 8kV Air +/-15kV Criteria: Class B	IEC61000-4-2			

10.1.5 Test Method



### 10.2 Inspection condition

10.2.1 Inspection conditions

10.2.1.1 Inspection Distance : 35 ± 5 cm

10.2.1.2 View Angle :

- (1) Inspection under operating condition :  $\pm 5^{\circ}$
- (2) Inspection under non-operating condition : ± 45°



10.2.2 Environment conditions :

Ambier	it Temperature :	25±5°C
Ambi	ent Humidity :	65±5%
Ambient	Cosmetic Inspection	400 ~ 600lux
Illumination	Functional Inspection	300 ~ 500lux

10.2.3 Definition of applicable Zones





No	Parameter	Criteria								
110.	T didificiei	Diaplay function: N		olfunction	A (Maior)					
		Display function. N	lo Display m	allunction	(iviajor)					
		Contrast ratio (Black, White):								
		Does not meet spe	ecified range		ec. (Iviajo	r (Note:3)	) 			
		Line Defect: No of and colored. (Majo	ovious Vertic or) (Note:1)	cal and Ho	orizontal	line defect	t in bright,	dark		
		Point Defect (Red, green, blue, dark): Active area ≤8dots (Minor)(Note:1								
		Item	Acceptable number	Total	CI	ass Of efects	AQL Level			
		Bright	3	6						
		Dark	5	0	r	Minor	15			
		Adjacent Bright	1	1			1.0			
		Adjacent Dark	2	2						
		Non-uniformity: Visible through 2%	ND filter wh	ite, R, G, I	B and gra	ay 50%pat	tern. (Mino	or)		
1	Operating	Foreign material in	Black or W	hite spots	shape (\	N>1/4L) (N	Note: 5)			
		Dimension		Acceptab	le Clas	ss Of	AQL			
				number	Def	ects	Level			
		D ≤ 0.5		 						
		0.5 < D ≤1.0		I	Vinor	1.5				
		D> 1.0	0	0						
		D = (Long + Short) / 2 * : Disregard								
		Foreign Material in Line or spiral shape (W≤1/4L) (Note: 4)								
		Dimer	Acc	Acceptable number		of AQL s Leve	.			
		W>0.3mm,L>10r		0						
		L≦10mm,0.2mm	n	4 Mir		1.5				
		L≦10mm,W≪0.:		*						
		L: Length W: W	Vidth *: [	Disregard						
		Dimension: Outline	e (Major)							
		Bezel appearance	: uneven (Mi	nor)						
		Scratch on the Pol	arize & Touc	<u>ch Panel :</u>	(Note:2)	010000		-		
		Dimen	sion	Acce nur	ptable nber	Defects	Level			
		W>0.3mm,L>10r	nm		0					
	External Inspection	L≦10mm,0.2mm	n <w≦0.3mm< td=""><td>n</td><td>4</td><td>Minor</td><td>1.5</td><td></td></w≦0.3mm<>	n	4	Minor	1.5			
2	(non-operating)	L≦10mm,W≤0.	2mm		*					
		L:Length W:W	Vidth *: [	Disregard				_		
		Dent and spots sh	ape on the p	olarize (N	ote:2): (N	Note: 5)				
		Dimens	sion	Accep num	table ber	Defects	Level			
		D ≤ 0.5		*						
		0.5 < D ≤1.0		4		Minor	1.5			
		D> 1.0		0						



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 D = (Long + Short) / 2 \* : Disregard

 D = (Long + Short) / 2 \* : Disregard

 Class of defects

 AQL 0.65
 It is a defect that is likely to result in failure or to reduce materially the usability of the product for the intended function.

 AQL 1.5
 It is a defect that will not result in functioning problem with deviation classified.

Note:1.(a)Bright point defect is defined as point defect of R,G,B with area >1/2 pixel respectively

(b)Dark point defect is defined as visible in full white pattern.

(c)The point defect must under 2% ND Filter visible .

Note:2 The external inspection should be conducted at the distance 30± 5cm between the eyes of inspector and the panel.

Note:3 Luminance measurement for contrast ratio is at the distance 50± 5cm between the detective

head and the panel with ambient luminance less than 1 lux. Contrast ratio is obtained at

optimum view angle. Note:4 W-Width in mm, L-length of Max.(L1,L2) in mm.



#### **10.4 Sampling Condition**

Unless otherwise agree in written, the sampling inspection shall be applied to the incoming inspection of customer.

Lot size: Quantity of shipment lot per model. Sampling type: normal inspection, single sampling Sampling table: ISO 2859

Inspection level: Level II



### **Product Label style:**



### **BarCode Define:**









#### 1. ASSEMBLY PRECAUTIONS

- (1) You must mount a module using holes arranged in four corners or four sides.
- (2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
- (4) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (5) Do not open the case because inside circuits do not have sufficient strength.
- (6) Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.
- (7) Please do not touch metal frames with bare hands and soiled gloves. A color change of the metal frames can happen during a long preservation of soiled LCD modules.
- (8) Please pay attention to handling lead wire of backlight so that it is not tugged in connecting with inverter.
- 2. OPERATING PRECAUTIONS
  - (1) Please be sure to turn off the power supply before connecting and disconnecting signal input cable.
  - (2) Please do not change variable resistance settings in LCD module. They are adjusted to the most suitable value. If they are changed, it might happen LCD does not satisfy the characteristics specification
  - (3) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
  - (4) When fixed patterns are displayed for a long time, remnant image is likely to occur.
  - (5) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
  - (6) Please consider that LCD backlight takes longer time to become stable of radiation characteristics in low temperature than in room temperature.
- 3. ELECTROSTATIC DISCHARGE CONTROL
  - (1) The operator should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such the copper leads on the PCB and the interface terminals with any parts of the human body.

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- (2) The modules should be kept in antistatic bags or other containers resistant to static for storage.
- (3) Only properly grounded soldering irons should be used.(4) If an electric screwdriver is used, it should be well arounded and shielded from commutator sparks.

 (5) The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended
 (6) Since dry air is inductive to statics, a relative humidit

(6) Since dry air is inductive to statics, a relative humidity of 50-60% is recommended.

#### 4. STORAGE PRECAUTIONS

- (1) When you store LCDs for a long time, it is recommended to keep the temperature between 0°C-40°C without the exposure of sunlight and to keep the humidity less than 90%RH.
- (2) Please do not leave the LCDs in the environment of high humidity and high temperature such as 60°C 90%RH
- (3) Please do not leave the LCDs in the environment of low temperature; below -20°C.
- 5. OTHERS
  - (1) A strong incident light into LCD panel might cause display characteristics' changing inferior because of polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight Land strong UV rays
  - (2) Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.
  - (3) For the packaging box, please pay attention to the followings:
  - a. Please do not pile them up more than 5 boxes. (They are not designed so.) And please do not turn over.
  - b. Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.
  - c. Packing box and inner case for LCDs are made of cardboard. So please pay attention not to get them wet. (Such like keeping them in high humidity or wet place can occur getting them wet.)
  - (4) Waste

Liquid crystal module products shall not be arbitrarily discarded, the water and soil have a negative impact on the environment, the need to be handled by a qualified unit.

6. LIMITED WARRANTY

Unless otherwise agreed between DATA IMAGE and customer, DATA IMAGE will replace or repair any of its LCD and LCM which is found to be defective electrically and visually when inspected in accordance with DATA IMAGE acceptance standards, for a period on one year from date of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of DATA IMAGE is limited to repair and/or replacement on the terms set forth above. DATA IMAGE will not responsible for any subsequent or consequential events.



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13. OUTLINE DRAWING





**14. PACKAGE INFORMATION** 

TBD



# DATA IMAGE CORPORATION

	TFT Module Specification ITEM NO.: <u>FG1001T0DSSWNG01</u> ■Prototype □Pre-prod. □Mass prod. Table of Contents	
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Customer Companies	QA Approval	QA Check	R&D Approval	R&D Check
	pretty	Andy	Dragon	Andrew
Approved by	Version:	Issued Date:	Total Pages::	Prepared by
	1	08/MAR/19'	28	Candy



### 2. RECORD OF REVISION

Rev	Date	Item	Page	Comment	Source
1	08/MAR/19'			Initial PRELIMINARY	ESR0802035



### **3. GENERAL SPECIFICATIONS**

Parameter	Specifications	Unit					
Screen Size	10.1 (diagonal)	inch					
Display resolution	1920(H) x (R,G,B) x 1200(V)	dot					
Active Area	216.81(H) × 135.5(V)	mm					
Pixel Pitch	0.1129(H) × 0.1129(V)	mm					
Pixel Arrangement	R.G.B. Vertical Stripe						
Outline Dimension	229.4(H) ×150(V) ×2.9(D)	mm					
Surface treatment	Glare						
Electrical Interface	MIPI						
Weight	TBD	g					
Display mode	AHVA, Normally Black						
our components and processes are con	our components and processes are compliant to RoHS standard						

### 4. ABSOLUTE MAXIMUM RATINGS

An absolute maximum rating of the module is as following:

### 4.1Absolute Ratings of TFT LCD Module

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Logic/LCD drive Voltage	Vin	-0.3	+4.5	[Volt]	Note 1,2

### **4.2Absolute Ratings of Environment**

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Operating Temperature	TOP	-10	+60	[°C]	
Operation Humidity	HOP	5	90	[%RH]	
Storage Temperature	TST	-20	+70	[°C]	
Storage Humidity	HST	5	90	[%RH]	

Note 1: At Ta (25°C)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: Maximum wet-bulb temperature is less than 39 °C and no condensation

Note 4: Operating temperature means "Front and rear surface" of panel

### 5. ELECTRICAL CHARACTERISTIC

### 5.1 TFT LCD Module

### 5.1.1 Power Specification

Input power specifications are as follows;

The power specification are measured under 25 and frame frequency under 60Hz

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
Logic/LCD Drive Voltage	VDD	3.0	3.3	4.2	[Volt]	
VDD Power	PDD	-	-	0.95	[Watt]	Note 1
IDD Current	IDD	-	-	316	[mA]	Note 1
Inrush Current	IRush	-	-	2000	[mA]	Note 2
Allowable Logic/LCD Drive Ripple Voltage	VDDrp	-	-	100	[mV] p-p	Note 2

Note 1 : Maximum Measurement Condition: White Pattern at 3.3V driving voltage. (Pmax=V3.3 x Iwhite)

Note 2: Measure Condition



### **VDD** rising time

**5.1.2 Signal Electrical Characteristics** Input signals shall be low or High-impedance state when VDD is off. MIPI DC/AC Characteristics are as follows;

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Input data bit rate	BRMIPI	200	-	1000	Mbps
Common-mode voltage(HS Rx mode)	VCMRX	70	-	330	mV
Differential input high threshold (HS Rx mode)	Vidth	-	-	70	mV
Differential input low threshold (HS Rx mode)	Vidtl	-70	-	-	mV
Differential input voltage range (HS Rx mode)	Vidm	70	-	500	mV
Single-end input high voltage (HS Rx mode)	VIHHS	-	-	460	mV
Single-end input low voltage (HS Rx mode)	VILHS	-40	-	-	mV
Differential input impedance	Zid	80	100	125	Ω
Logic 1 input voltage (LP Rx mode)	Vihlp	880			mV
Logic 0 input voltage (LP Rx mode)	VILLP			550	mV
Output high level (LP Tx mode)	Vон	1.08	1.2	1.32	V
Output low level (LP Tx mode)	Vol	-50		50	mV







HS Differential Signaling

LP Single-ended Signaling

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Common-mode interference beyond 450MHz	$\triangle V_{CMRX(HF)}$		-	-	100	mV
Common-mode interference 50MHz ~ 450MHz	$\triangle V_{CMRX(LF)}$		-50	-	50	mV
Common-mode termination	Ссм		-	-	60	pF
UI instantaneous	UIINST		1	-	12.5	ns

HS RX Scheme





Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Notes
Data to Clock Skew (mesured at transmitter)	Tskew[tx]	-0.15	-	0.15	UIINST	Note1
Data to Clock Setup Time (receiver)	TSETUP[RX]	0.15		-	UIINST	Note2
Data to Clock Hold Time (receiver)	THOLD[RX]	0.15	-	-	UIINST	Note2

Note:

1. Total silicon and package delay budget of 0.3\*UIINST

2. Total setup and hold window for receiver of 0.3\*UINST

High Speed Data Transmission: Data to Clock Timing



Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input pulse rejection	<b>E</b> SPIKE		-	-	300	V.ps
Minimum pulse width response	Tmin-rx		50	-	-	ns
Peak interference amplitude	Vint		-	-	200	mV
Interference frequency	fint		450	-	-	MHz

Input Glitch Rejection of Low-Power Receivers



For MIPI data transmission from TX to TCON works properly in video mode, it is suggested that all of MIPI

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lanes

status follow the scheme showed in below. When power is turned on, all lanes (include clock lane) are into LP-11

status first. When TX wants to start transmitting data to TCON, the clock lane is into HS and start toggling. Then data

lanes are into HS and data are transmitted. After data transmissions are finished (ex. H-blanking, V-blanking), the

data lanes are returned to LP-11, then clock lane, too. The transmission start from LP-11 and stop in LP-11 on all

lanes (include clock lane) are the recommended proper operation sequence for MIPI video mode.



#### The timing definitions are listed in below,

Parameter Description		MIN.	TYP.	MAX.	Unit
TCLK-MISS Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.				60	ns
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has DST transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.				ns
Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.		8			UI
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
TCLK-SETTLE	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.	95		300	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.			38	ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
TCLK-PREPARE + time that the + TCLK-ZERO TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.		300			ns
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time			35 ns + 4*UI	ns

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	point when				
	Dn crosses VIL,MAX.				
TEOT Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst.				105 ns + 12*UI	ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	100			ns
THS-SYNC	HS Sync-Sequence '00011101' period		8		UI
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + 4*UI		85 ns + 6*UI	ns
THS-PREPARE + THS-ZERO	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI			ns
THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE.	85 ns + 6*UI		145ns + 10*UI	ns
THS-SKIP	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55 ns + 4*UI	ns
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60 ns + 4*UI			ns
TLPX	Transmitted length of any Low-Power state period	50			ns
Ratio TLPX	Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	2/3		3/2	
TTA-GET	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	5*TLPX			ns
TTA-GO	Time that the transmitter drives the Bridge state(LP-00) before releasing control during a Link Turnaround.		4*TLPX		ns
TTA-SURE	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX		2*TLPX	ns

Note:

2. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

High-Speed Data Transmission in Bursts

<sup>1.</sup> The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.



Switching the Clock Lane between Clock Transmission and Low-Power Mode



**Turnaround Procedure** 



### 5.2 Backlight Unit 5.2.1 LED characteristics

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Backlight Power Consumption	PLED	-	-	4.9	[Watt]	(Ta=25℃ @800nits)
LED Life-Time	N/A	15,000	20,000	-	Hour	(Ta=25℃ @800nits) Note1
LED Forward Voltage	VF	5.5	5.65	5.8	[Volt]	(Ta=25℃)
LED Forward Voltage of every LED string	VF-string	-	-	34.8	[Volt]	(Ta=25℃) Note2
LED Forward Current	IF	-	20	-	[mA]	(Ta=25℃)

Note 1. The LED life-time define as the estimated time to 50% degradation of initial luminous.

Note2. LED Array 6 parallel \* 6 series

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Remark
LED Power Supply	VLED	3		12	[Volt]	
LED Enable Input High Level		1.7	-	5.5	[Volt]	
LED Enable Input Low Level	VLED_EN	-	-	0.8	[Volt]	Define as Connector
PWM Logic Input High Level	VPWM_E	1.7	-	5.5	[Volt]	Interface (Ta=25℃)
PWM Logic Input Low Level	N	-	-	0.8	[Volt]	Note1
PWM Input Frequency	FPWM	200	-	10K	Hz	
PWM Duty Ratio	Duty	1		100	%	

### 5.2.2 Backlight input signal characteristics

Note 1: The input high level voltage conversion to 2.5V by level shift circuit. Note 2: The LED PWM Logic Input Low Level Voltage must have an output impedance close to 0 ohm in front of input connector.



### 6. INPUT SIGNAL CHARACTERISTICS

### 6.1 Timing Characteristics

Basically, interface timings should match the 1920x1200 /60Hz manufacturing guide line timing.

P	arameter	Symbol	MIN.	TYP.	MAX.	Unit
Frame Rate		-	-	60	-	Hz
Clock frequency		1/ TClock	148.04	149.9	151.27	MHz
Vertical Section	Period	T∨	1206	1212	1218	
	Active	Tvd		TLine		
	Blanking	Тув	6	12	18	
Horizontal Section	Period	Тн	2046	2058	2070	
	Active	Тно	1920			TClock
	Blanking	Тнв	126	138	150	

Note : DE mode only

### 6.1.2 Timing diagram



### 6.2 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.





Power Sequence Timing					
Denemeter	Va	lue	Units		
Parameter	MIN.	MAX.	01113		
T1	0.5	10			
T2	40	-			
T5	120	-			
Т6	50	-			
T7	0	-			
Т8	0	10			
T11	500	-	1115		
T12	10	-			
T13	10	-			
T14	0.5	10			
T15	10	-			
T18	10	-			

Note: LED\_PWM must be pull low(GND) when it is not pull high.

### 6.3 Signal Interface Characteristic 6.3.1 Pixel Format Image

Following figure shows the relationship between input signal and LCD pixel format.





### 6.3.2 The Input Data Format

Input Pixel Stream Format (1920RGB in 4 Lanes with RGB 8-8-8 format)



LPS : Low Power State

SoT : Start of Transmission

EoT : End of Transmission

ECC : Error-Correcting Code

### 6.4 Integration Interface Requirement

### 6.4.1 MIPI Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

<b>Connector Name / Designation</b>	For Signal Connector
Manufacturer	HIROSE
Type / Part Number	FH34SJ-34S-0.5SH(50) or compatible
Mating Housing/Part Number	FPC Cable



### 7. OPTICAL CHARACTERISTIC

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks	
	[degree]	Horizontal (Right) CR = 10 (Left)	80	85	-			
Viewing Angle	[degree]	Horizontal (Right) CR = 10 (Left)	80	85	-	dog	Note 1.4	
(CR≥10)	[degree]	Vertical (Upper) CR = 10 (Lower)	80 85 - deg	ueg	NOLE 1,4			
	[degree]	Vertical (Upper) CR = 10 (Lower))	80	85	-			
Contrast Ratio	CR	Normal	600	800	-		Note 1,3	
Response time	Ton	θ=Φ=0°	-	25	35	ms	Note 1,6	
	Red x		TBD	TBD	TBD	-	Note 1.7	
	Red y		TBD	TBD	TBD	-		
	Green x		TBD	TBD	TBD			
Color chromaticity	Green y		TBD	TBD	TBD			
Color enronnationly	Blue x		TBD	TBD	TBD			
	Blue y		TBD	TBD	TBD			
	White x		TBD	TBD	TBD			
	White y		TBD	TBD	TBD			
Luminance	L		600	800	-	Cd/m <sup>²</sup>	Note 1,2	
Luminance uniformity	B-uni	5 points	70		-	%	Note1,5	
Image sticking		tis			2	Sec	Note 8	

The following optical specifications shall be measured in a darkroom or equivalent state (ambient luminance  $\leq 1$  lux, and at room temperature). The operation temperature is  $25^{\circ}C\pm 2^{\circ}C$ . The measurement method is shown in Note1.

Note1: The method of optical measurement:



Note2: Measured at the center area of the panel and at the viewing angle of the  $\theta x=\theta y=0^{\circ}$ Note3: Definition of Contrast Ratio (CR):

CR = Luminance with all pixels in white state Luminance with all pixels in Black state

Note4: Definition of Viewing Angle





#### Note 5: Definition of Brightness Uniformity (B-uni):





Note6: Definition of Response Time:

The Response Time is set initially by defining the "Rising Time (Tr)" and the "Falling Time (Tf)" respectively. Tr and Tf are defined as following figure.



 Image
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 Data input
 White
 Black
 White

 Image
 Image
 Image
 Image
 Image

 Image
 Image
 Image
 Image
 Image

Note 7: Definition of Chromaticity:

The color coordinates  $(x_W, y_W), (x_R, y_R), (x_G, y_G)$ , and  $(x_B, y_B)$  are obtained with all pixels in the viewing field at white, red, green, and blue states, respectively.

Note 8: Definition of Image sticking (tis):

Continuously display the test pattern shown in the figure below for 2 hours. Then display a completely white screen. The previous image shall not persist more than 2 sec at 25 °C





Pin No	Symbol	Function	Remark
1	VDD	DC-DC circuit supply voltage	
2	VDD	DC-DC circuit supply voltage	
3	Hsync	Yoe signal output to system	
4	LED_EN	LED driver Enable Input	
5	LED_PWM	Backlight LED driver PWM Input	
6	ID	Pull high (10Kohm to 1.8V)	
7	ID	Pull high (10Kohm to 1.8V)	
8	NC	Not Connection	
9	GND	Ground	
10	DSI_D2P/Rx-IN2P	MIPI data pair 2 positive signal	
11	DSI_D2N/Rx-IN2N	MIPI data pair 2 negative signal	
12	GND	Ground	
13	DSI_D1P/Rx-IN1P	MIPI data pair 1 positive signal	
14	DSI_D1N/Rx-IN1N	MIPI data pair 1 negative signal	
15	GND	Ground	
16	DSI_CLKP/Rx-CLKP	MIPI Clock positive signal	
17	DSI_CLKN/Rx-CLKN	MIPI Clock negative signal	
18	GND	Ground	
19	DSI_D0P/Rx-IN0P	MIPI data pair 0 positive signal	
20	DSI_D0N/Rx-IN0N	MIPI data pair 0 negative signal	
21	GND	Ground	
22	DSI_D3P/Rx-IN3P	MIPI data pair 3 positive signal	
23	DSI_D3N/Rx-IN3N	MIPI data pair 3 negative signal	
24	GND	Ground	
25	GND	Ground	
26	GND	Ground	
27	GND	Ground	
28	ID	Pull low (4.7Kohm to Ground)	
29	Aging	Aging Mode Power Supply (AUO only)	
30	NC	Not Connection	



31	LED+	LED Power Supply	
32	LED+	LED Power Supply	
33	LED+	LED Power Supply	
34	LED+	LED Power Supply	







### 10.1 Test Condition

- 10.1.1 Temperature and Humidity(Ambient Temperature)
  - Temperature :  $25 \pm 5^{\circ}C$ Humidity :  $65 \pm 5\%$
- 10.1.2 Operation

Unless specified otherwise, test will be conducted under function state.

### 10.1.3 Container

Unless specified otherwise, vibration test will be conducted to the product itself without putting it in a container.

### 10.1.4 Test Frequency

In case of related to deterioration such as shock test. It will be conducted only once.

	Reliability Test Item & Level						
No.	Item	Test Conditions	Remark				
1	High Temperature Storage Test	Ta = 70°C 300Hr	IEC60068-2-2				
2	Low Temperature Storage Test	Ta = -20℃ 300Hr	IEC60068-2-1				
3	High Temperature Operation Test	Ts = 60°C 300Hr	IEC60068-2-2				
4	Low Temperature Operation Test	Ta = -10℃ 300Hr	IEC60068-2-1				
5	Operate at High Temperature and Humidity	40 °C /90%,300Hr	IEC60068-2-3				
6	Thermal Shock	-10 ℃ /30 min , 60 ℃ /30 min , 20cycles	IEC60068-2-14				
7	Vibration Test	Acceleration: 1.5 G Frequency: 10 - 500Hz Random Sweep: 30 Minutes each Axis (X, Y, Z) Test method: Non-Operation	IEC60068-2-6				
8	Drop test (Package)	Height :60cm 1 conner,3edges,6surfaces	IEC60068-2-32				
9	ESD	State: operating Location: LCM/TP surface Condition:150pf 330Ω Contact +/- 8kV Air +/-15kV Criteria: Class B	IEC61000-4-2				

#### 10.1.5 Test Method



### 10.2 Inspection condition

10.2.1 Inspection conditions

10.2.1.1 Inspection Distance : 35 ± 5 cm

10.2.1.2 View Angle :

- (1) Inspection under operating condition :  $\pm 5^{\circ}$
- (2) Inspection under non-operating condition : ± 45°



10.2.2 Environment conditions :

Ambier	it Temperature :	25±5°C
Ambi	ent Humidity :	65±5%
Ambient	Cosmetic Inspection	400 ~ 600lux
Illumination	Functional Inspection	300 ~ 500lux

10.2.3 Definition of applicable Zones





No.0 II	Parameter	Criteria						
110.	T diameter	Display function: No Display malfunction (Major)						
	Operating							
		Contrast ratio (Black, White):						
		Does not meet specified range in the spec. (Major) (Note:3)						
		Line Detect: No obvious Vertical and Horizontal line detect in bright, dark and colored. (Major) (Note:1)						
		Point Defect (Red, green, blue, dark): Active area ≤8dots (Minor)(Note:1)						
		Item	Acceptable number	Total	Cla De	ass Of efects	cts Level	
		Bright	3	6				
		Dark	5	0	Minor		1.5	
		Adjacent Bright	1	1			1.0	
		Adjacent Dark	2	2				
		Non-uniformity: Visible through 2%ND filter white, R, G, B and gray 50%pattern. (Minor)						
1		Foreign material in	hite spots sha	e spots shape (W>1/4L) (Note: 5)				
		Dimension		Acceptable	Class Of		AQL	
				number	Defe	Defects Level		
		D ≤ 0.5		<u> </u>	4			
		0.5 < D ≤1.0 D> 1.0		-	Minor		1.5	
				0				
		D = (Long + Short) / 2 * : Disregard						
		Foreign Material in Line or spiral shape (W≤1/4L) (Note: 4)						
		Dimension		Accept numl	Acceptable number		cts Level	
		W>0.3mm,L>10r	0	)				
		$L \leq 10$ mm,0.2mm< $W \leq 0.3$ mm		n 4	4 M		or 1.5	
		L≦10mm,W≤0.2mm *						
		L : Length W : Width * : Disregard						
	External Inspection (non-operating)	Dimension: Outline (Major)						
		Bezel appearance: uneven (Minor)						
2		Scratch on the Polarize & Touch Panel : (Note:2)						
		Dimension		Accepta numbe	bie er	Defects	Level	
		W>0.3mm,L>10mm		0				
		$L \leq 10$ mm,0.2mm< $W \leq 0.3$ mm		n <sup>4</sup>		Minor	1.5	
		L≦10mm,W≪0.	*					
		L: Length W: Width *: Disregard						
		Dent and spots sha	olarize (Note	:2): (N	Note: 5) Class Of $\Delta OI$		1	
		Dimension		number	e Class Of Defects		Level	
		$D \le 0.5$		*				
		0.5 < D ≤1.0		4		Minor	1.5	
		D> 1.0		0				



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 D = (Long + Short) / 2 \* : Disregard

 D = (Long + Short) / 2 \* : Disregard

 Class of defects

 AQL 0.65
 It is a defect that is likely to result in failure or to reduce materially the usability of the product for the intended function.

 AQL 1.5
 It is a defect that will not result in functioning problem with deviation classified.

Note:1.(a)Bright point defect is defined as point defect of R,G,B with area >1/2 pixel respectively

(b)Dark point defect is defined as visible in full white pattern.

(c)The point defect must under 2% ND Filter visible .

Note:2 The external inspection should be conducted at the distance 30± 5cm between the eyes of inspector and the panel.

Note:3 Luminance measurement for contrast ratio is at the distance 50± 5cm between the detective

head and the panel with ambient luminance less than 1 lux. Contrast ratio is obtained at

optimum view angle. Note:4 W-Width in mm, L-length of Max.(L1,L2) in mm.



#### **10.4 Sampling Condition**

Unless otherwise agree in written, the sampling inspection shall be applied to the incoming inspection of customer.

Lot size: Quantity of shipment lot per model. Sampling type: normal inspection, single sampling Sampling table: ISO 2859

Inspection level: Level II



### **Product Label style:**



### **BarCode Define:**









#### 1. ASSEMBLY PRECAUTIONS

- (1) You must mount a module using holes arranged in four corners or four sides.
- (2) You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.
- (3) Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment.
- (4) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.
- (5) Do not open the case because inside circuits do not have sufficient strength.
- (6) Please do not take a LCD module to pieces and reconstruct it. Resolving and reconstructing modules may cause them not to work well.
- (7) Please do not touch metal frames with bare hands and soiled gloves. A color change of the metal frames can happen during a long preservation of soiled LCD modules.
- (8) Please pay attention to handling lead wire of backlight so that it is not tugged in connecting with inverter.
- 2. OPERATING PRECAUTIONS
  - (1) Please be sure to turn off the power supply before connecting and disconnecting signal input cable.
  - (2) Please do not change variable resistance settings in LCD module. They are adjusted to the most suitable value. If they are changed, it might happen LCD does not satisfy the characteristics specification
  - (3) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
  - (4) When fixed patterns are displayed for a long time, remnant image is likely to occur.
  - (5) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
  - (6) Please consider that LCD backlight takes longer time to become stable of radiation characteristics in low temperature than in room temperature.
- 3. ELECTROSTATIC DISCHARGE CONTROL
  - (1) The operator should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such the copper leads on the PCB and the interface terminals with any parts of the human body.

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- (2) The modules should be kept in antistatic bags or other containers resistant to static for storage.
- (3) Only properly grounded soldering irons should be used.(4) If an electric screwdriver is used, it should be well arounded and shielded from commutator sparks.

 (5) The normal static prevention measures should be observed for work clothes and working benches; for the latter conductive (rubber) mat is recommended
 (6) Since dry air is inductive to statics, a relative humidit

(6) Since dry air is inductive to statics, a relative humidity of 50-60% is recommended.

#### 4. STORAGE PRECAUTIONS

- (1) When you store LCDs for a long time, it is recommended to keep the temperature between 0°C-40°C without the exposure of sunlight and to keep the humidity less than 90%RH.
- (2) Please do not leave the LCDs in the environment of high humidity and high temperature such as 60°C 90%RH
- (3) Please do not leave the LCDs in the environment of low temperature; below -20°C.
- 5. OTHERS
  - (1) A strong incident light into LCD panel might cause display characteristics' changing inferior because of polarizer film, color filter, and other materials becoming inferior. Please do not expose LCD module direct sunlight Land strong UV rays
  - (2) Please pay attention to a panel side of LCD module not to contact with other materials in preserving it alone.
  - (3) For the packaging box, please pay attention to the followings:
  - a. Please do not pile them up more than 5 boxes. (They are not designed so.) And please do not turn over.
  - b. Please handle packaging box with care not to give them sudden shock and vibrations. And also please do not throw them up.
  - c. Packing box and inner case for LCDs are made of cardboard. So please pay attention not to get them wet. (Such like keeping them in high humidity or wet place can occur getting them wet.)
  - (4) Waste

Liquid crystal module products shall not be arbitrarily discarded, the water and soil have a negative impact on the environment, the need to be handled by a qualified unit.

6. LIMITED WARRANTY

Unless otherwise agreed between DATA IMAGE and customer, DATA IMAGE will replace or repair any of its LCD and LCM which is found to be defective electrically and visually when inspected in accordance with DATA IMAGE acceptance standards, for a period on one year from date of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of DATA IMAGE is limited to repair and/or replacement on the terms set forth above. DATA IMAGE will not responsible for any subsequent or consequential events.



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13. OUTLINE DRAWING





**14. PACKAGE INFORMATION** 

TBD